Integrated Quantum Information Platforms at MIT Lincoln Laboratory

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NY Creates Seminar

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LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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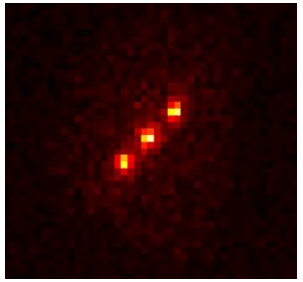
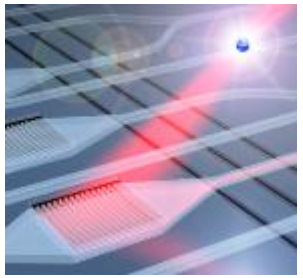
Outline

- **Platforms for quantum information processing**
- **Trapped-ion quantum computing and sensing**
  - **Concept for trap array with integrated controls**
- **Integrated Photonics Development**
  - **Visible platform: Al_2O_3/PECVD SiN (low loss, multi-layer, CMOS-compatible)**
  - **Ion operations with multiple wavelengths of light, on-chip**
  - **Expanded photonics platform: potential for enhanced QIP functionality**
- **Integrated Electronics**
  - **Monolithic integration of electronic controls for trapped ions**
  - **Photon detection and 3D integration**
- **Near-Term Collaborations Utilizing the Ion Platform**





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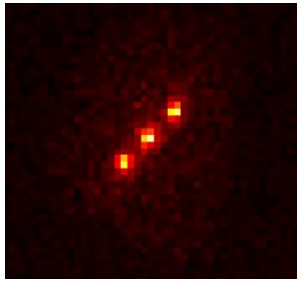
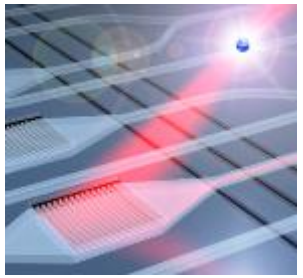
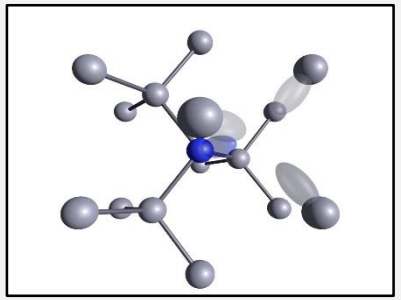


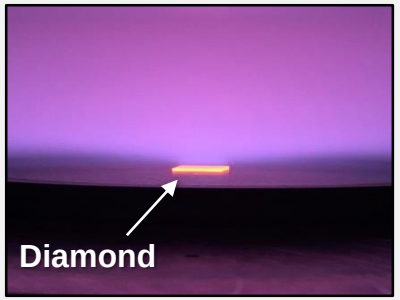


MIT-LL Diamond Quantum Systems Seed Applications

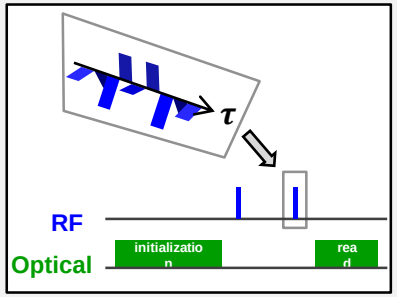
Quantum System Design



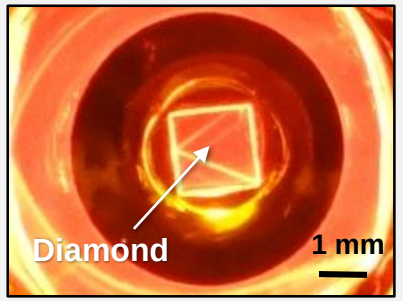
Diamond Growth and Fabrication



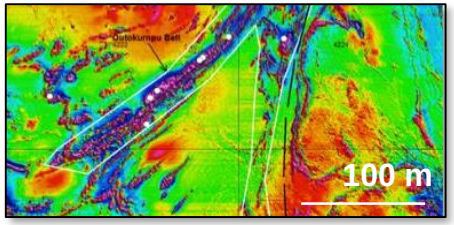
Quantum Control



Diamond Devices

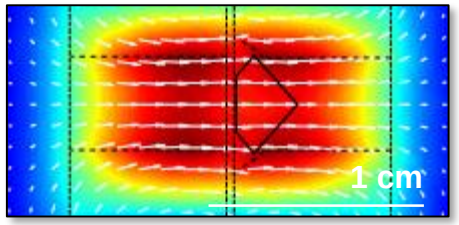


Magnetic-Assisted Navigation & Mapping



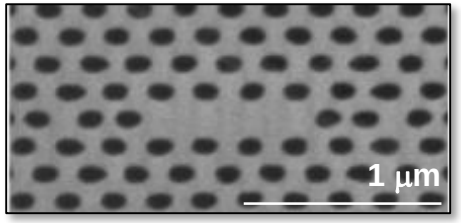
Nitrogen vacancy diamond magnetometers improve navigation without GPS

Small SWaP Devices by Quantum Engineering



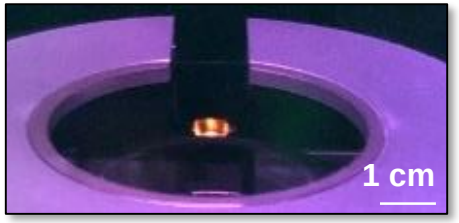
Cavity readout of diamond and alternate solid-state materials opens new class sensors

Quantum Networks



Silicon vacancy defect centers in diamond enable scalable quantum memories, a core element of networks

Magnetic Imaging Applications

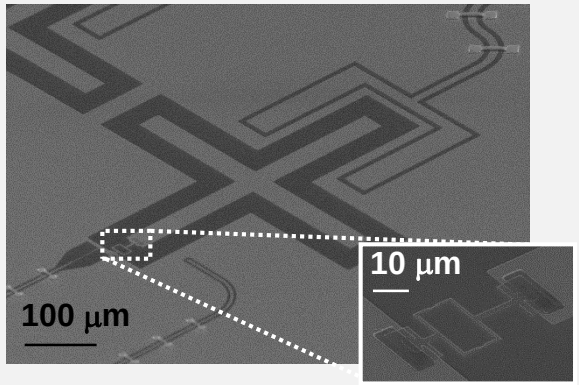


Quantum-grade "diamond magnetic microscope" enables high spatial resolution magnetic imaging

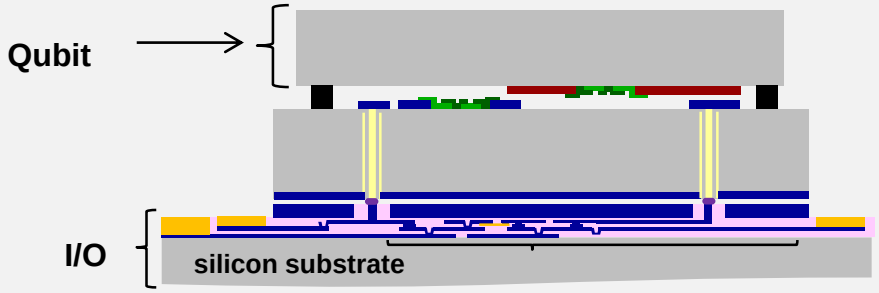
Connecting quantum diamond development with system-level applications enables new sensing paradigms

MIT-LL Superconducting Qubit Platform

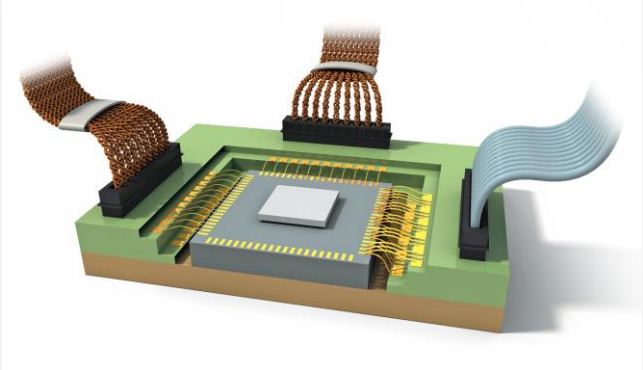
Circuit-Based Artificial Atoms



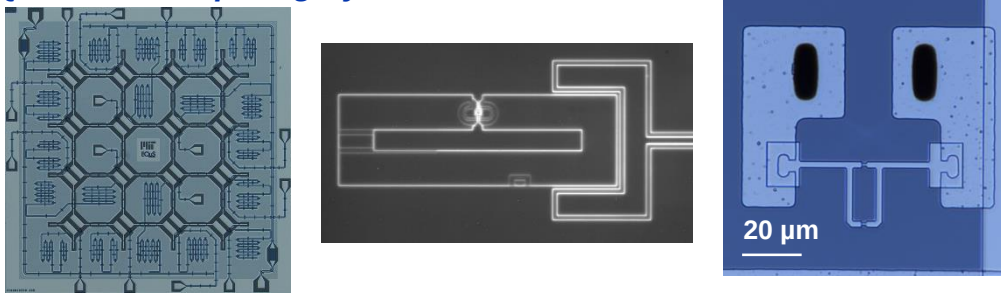
Three Dimensional Integration



Quantum Superconducting Platform

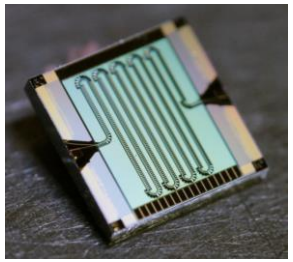


Quantum Computing Systems



Superconducting qubits in planar, flip-chip, and thru-silicon via integrated modalities

Enabling Community

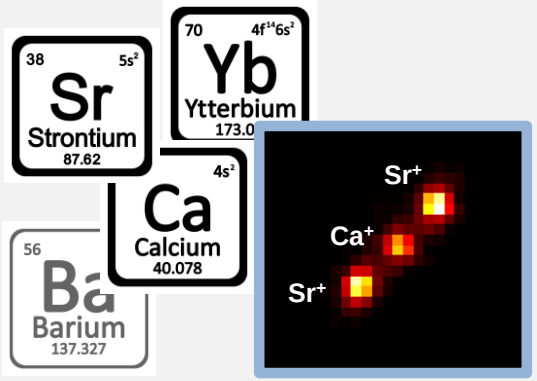


Providing amplifiers and quantum processors to academic, industry, and national laboratory partners

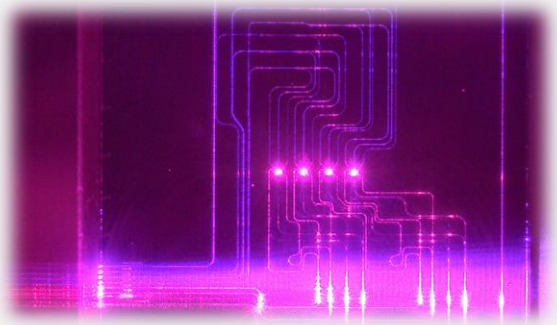
Superconducting quantum computing investment has enabled robust external programs pursuing next generation quantum computing and enabling the broader community

MIT-LL Atomic / Ion Quantum Platform

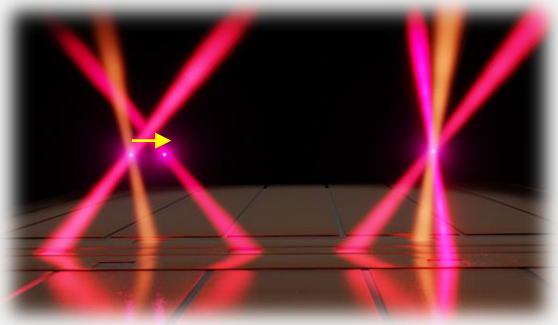
Multi-Ion Quantum Systems



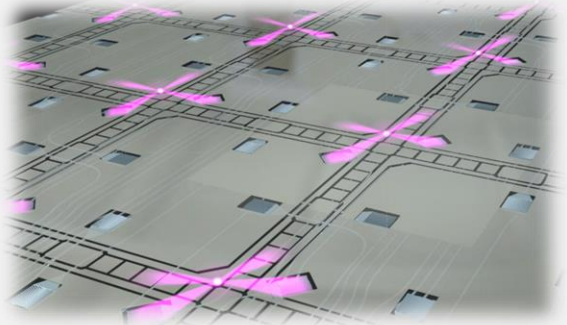
Integrated Chip-Based Trapping



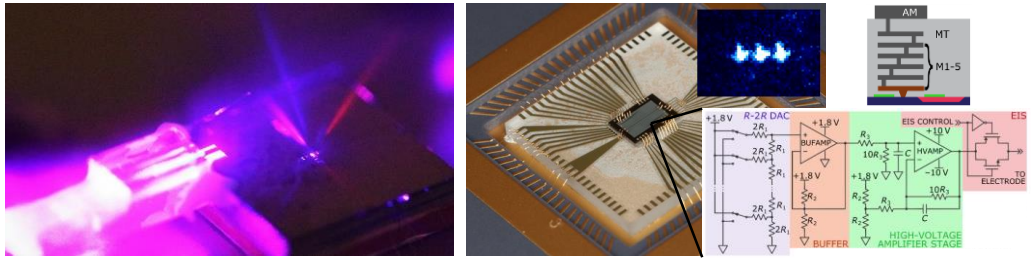
Quantum Computing & Sensing



Advanced Multi-Zone Quantum Control

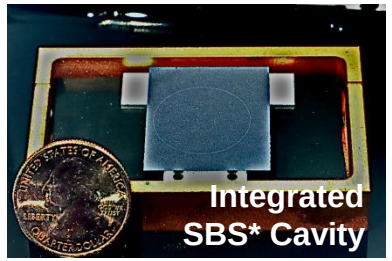


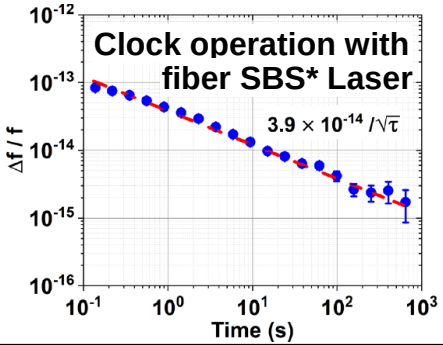
Robust Trapped-Ion Quantum Computing



Ion platforms with in-chip routing of optical and electronic control signals

Chip-based Optical Clocks





First demonstration of an integrated chip optical clock controlled by a compact stimulated Brillouin scattering (SBS) laser.

Integrated ion platform enables core mission areas of advanced quantum computing and portable precision timing and collaborations through the National Quantum Initiative

*SBS: stimulated Brillouin scattering

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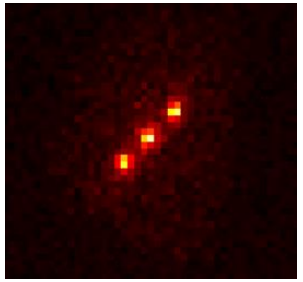
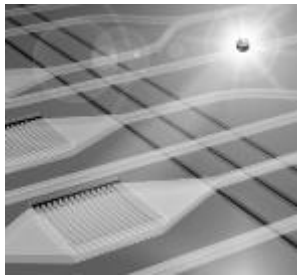
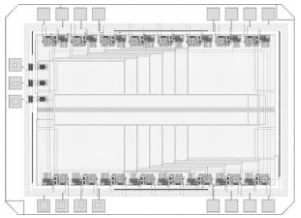


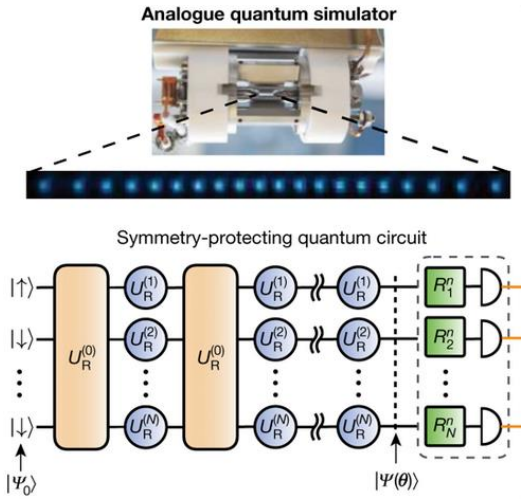




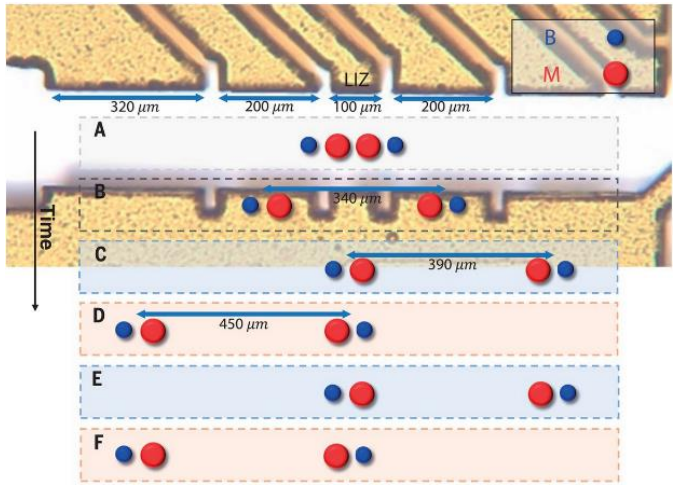
Trapped-Ion Quantum Computing with Ions

Complex qubit organization: each row is a separate image of 53 trapped ion qubits, with each qubit fluorescing (state 1) or dark (state 0) upon measurement.,

Zhang et al., Nature (2017)

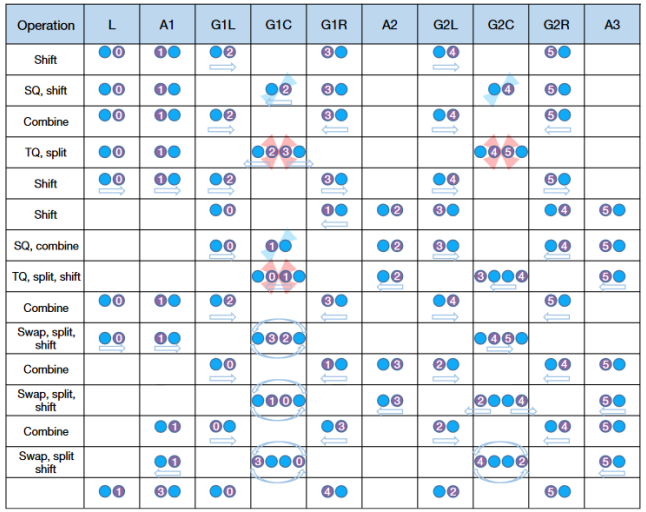


Kokail et al., Nature (2019)



Wan et al., Science (2019)

- 53-qubit quantum sim. with indiv. ion-qubit control (UMD)
- Programmable, verifiable 20-qubit quantum sim. (Innsbruck)
- Quantum simulation of water molecule (IonQ/UMD)
- Gate teleportation between separated qubits (NIST)
- Six-qubit arrayed-architecture/motion demo (HQS)
- Two-qubit gates >99.9% fid. (NIST) and 99.8%, 1.6 us (Oxford)



Pino et al., Nature (2021)

Ions as Sensors: Very Good Clocks

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Viewpoint: Ion Clock Busts into New Precision Regime

Pierre Dubé, National Research Council of Canada, Ottawa, Ontario

July 15, 2019 • *Physics* 12, 79

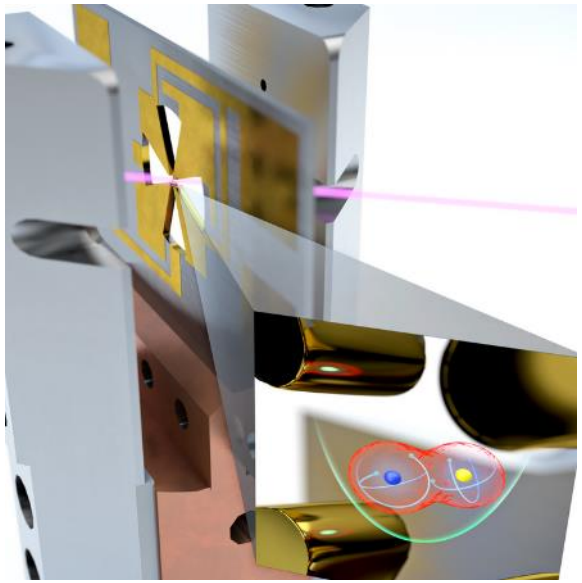
An aluminum ion clock has a fractional-frequency uncertainty of less than one part in 10^{18}, a four-decades-long goal in precision.

PDF Version Print

$^{27}Al^{+}$ Quantum-Logic Clock with a Systematic Uncertainty below 10^{-18}

S. M. Brewer, J.-S. Chen, A. M. Hankin, E. R. Clements, C. W. Chou, D. J. Wineland, D. B. Hume, and D. R. Leibrandt

Phys. Rev. Lett. 123, 033201 (2019)
Published July 15, 2019



- **Currently, the best clock in the world: a single Al^{+} ion controlled via a single Mg^{+} ion using quantum logic**
  - **Fractional frequency uncertainty below 10^{-18} (1 s in 33 billion yr)**
  - **Sensitive to gravitational redshift at the few-cm level**
  - **More precise than best lattice clocks (but not more stable, due to fewer atoms)**
- **Enables not only precision timing but basic science**

Trapped-Ion Qubit Approach

Ion

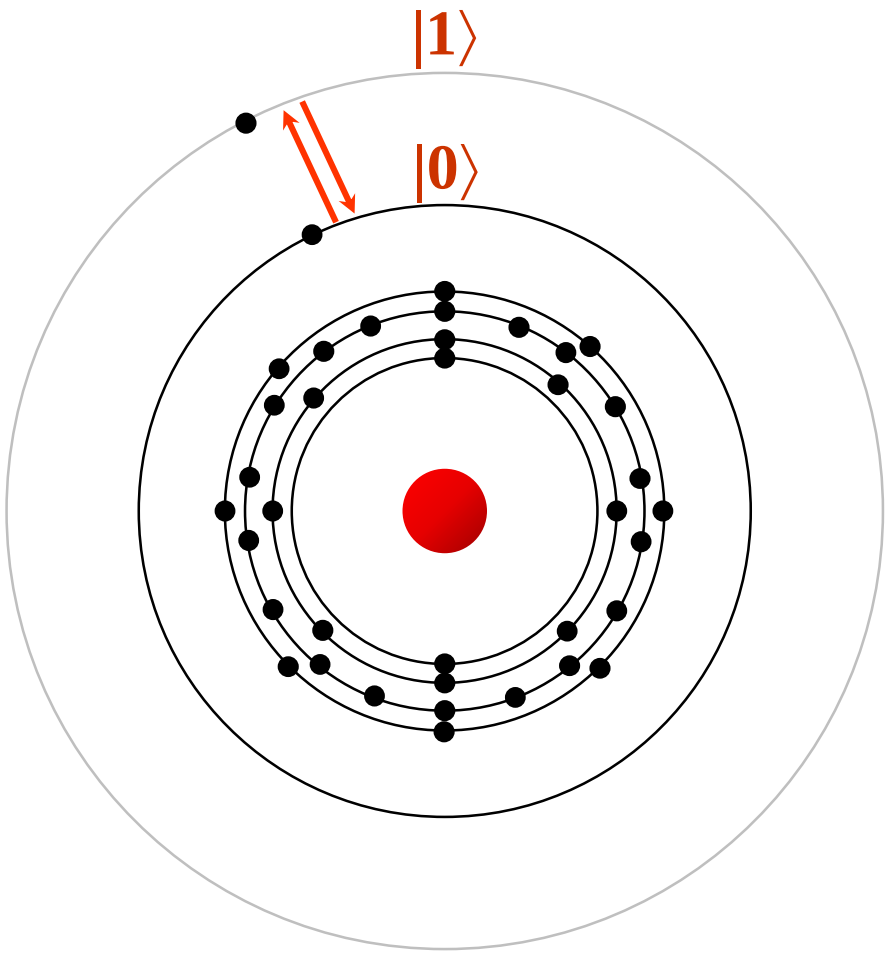
- Utilize Sr atom with one electron removed (Sr^+)

Qubit State

- Utilize state of outermost electron (Ground vs. Metastable excited state)

Ion Trapping

- Oscillating quadrupole field confines ion



Sr^+ ion

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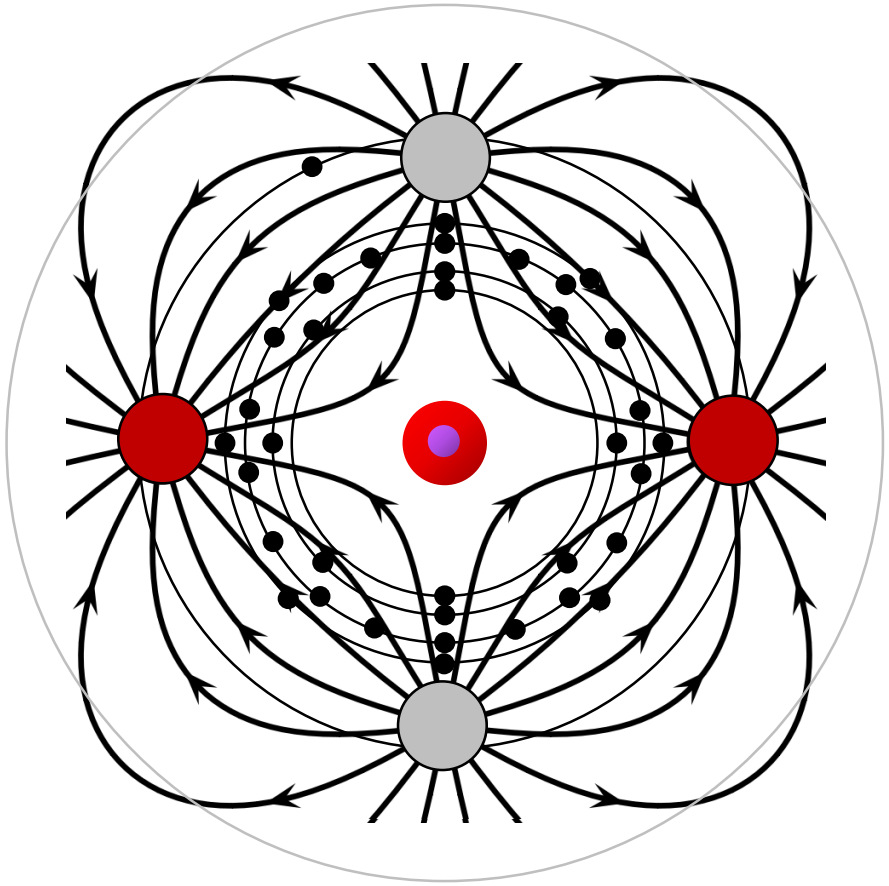
"Bulk" linear Paul Trap (PTB)

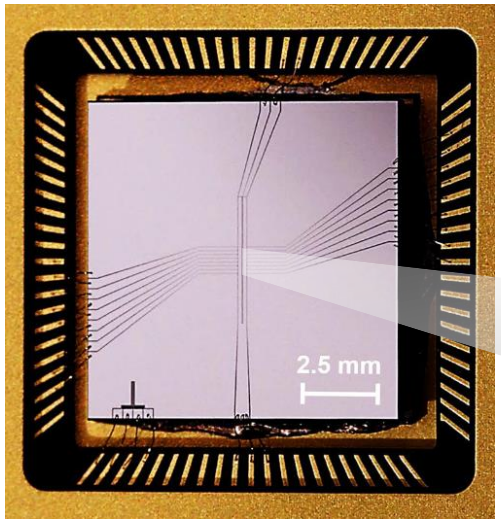


Sr^+ ion

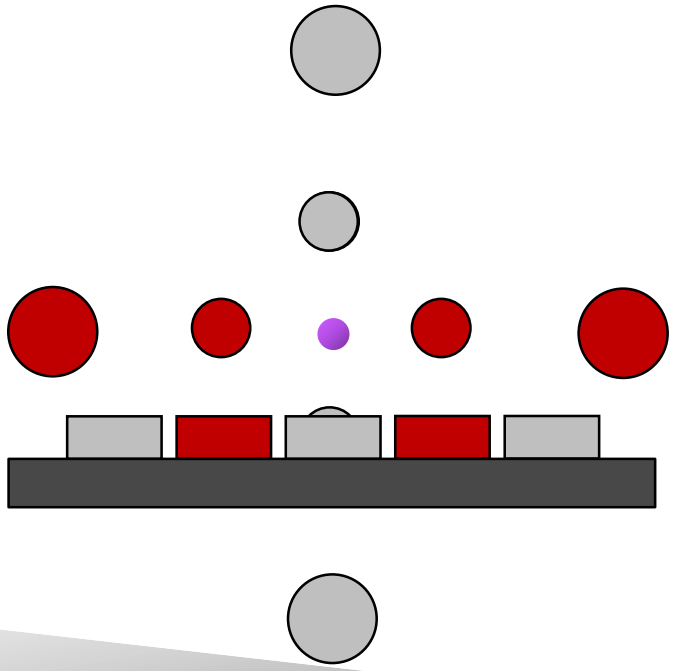
Surface Electrode Ion Traps

Shrinking and Planarizing the Four-Rod Geometry

- **Quadrupole unfolded into a plane**
- **Produces an effective 3D harmonic well above the chip surface**

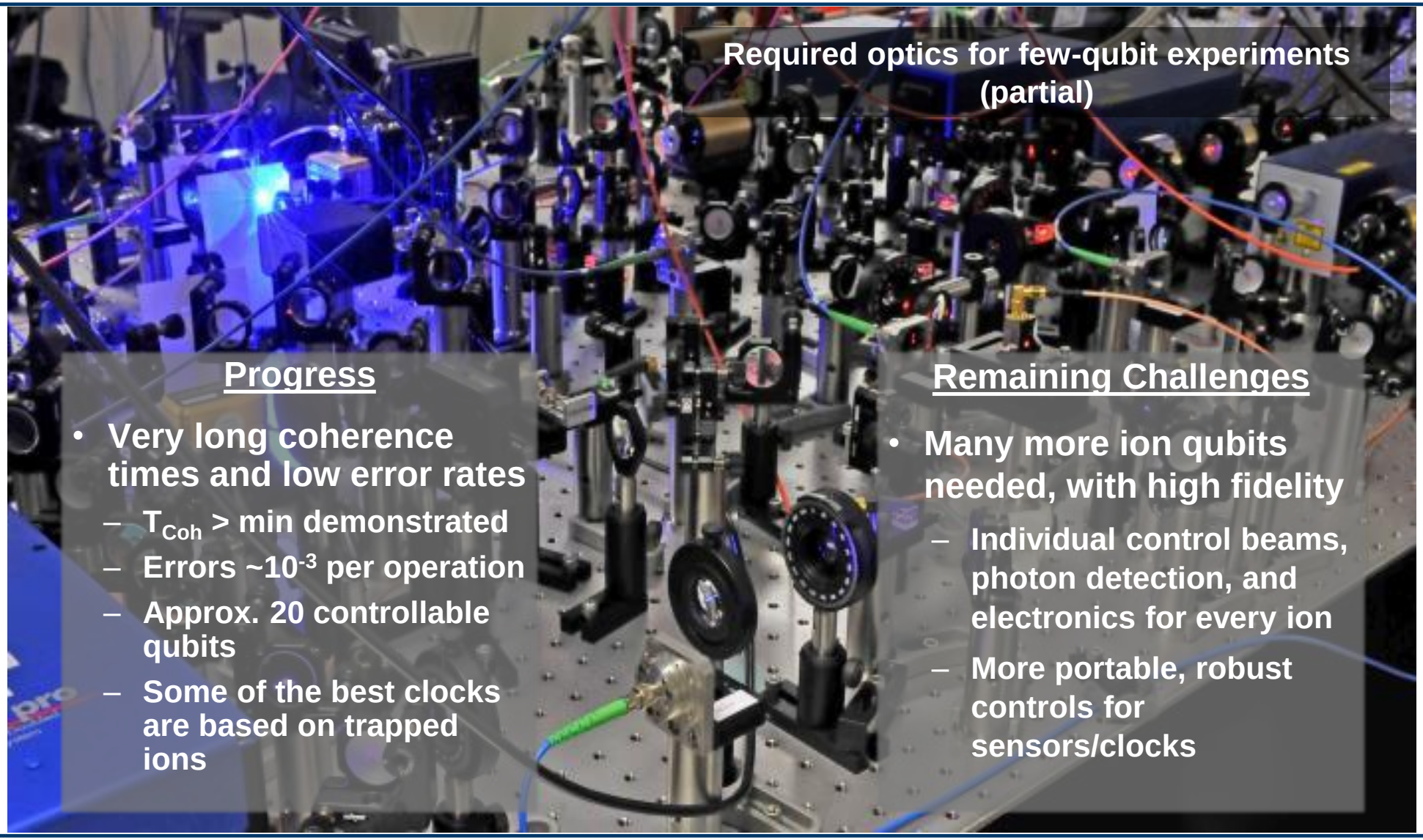


Surface electrode linear Paul trap (MIT LL)



Sr^+ ions, 50 um from trap surface, and approximately 5 um apart

Trapped Ion Quantum Information Processing Progress & Challenges



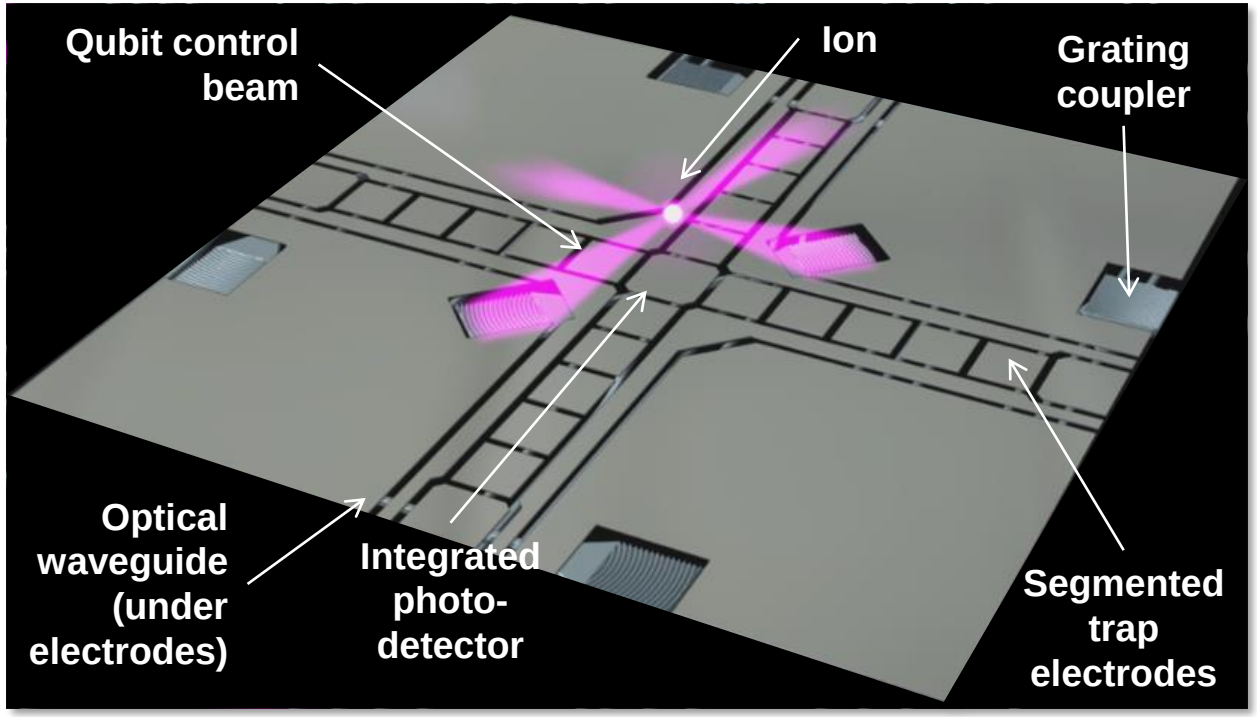
Progress

- Very long coherence times and low error rates
  - T_{Coh} > min demonstrated
  - Errors ~10^{-3} per operation
  - Approx. 20 controllable qubits
  - Some of the best clocks are based on trapped ions

Remaining Challenges

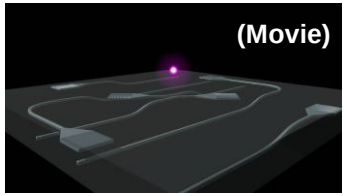
- Many more ion qubits needed, with high fidelity
  - Individual control beams, photon detection, and electronics for every ion
  - More portable, robust controls for sensors/clocks

Potential Quantum Computing/Sensing Array Cell



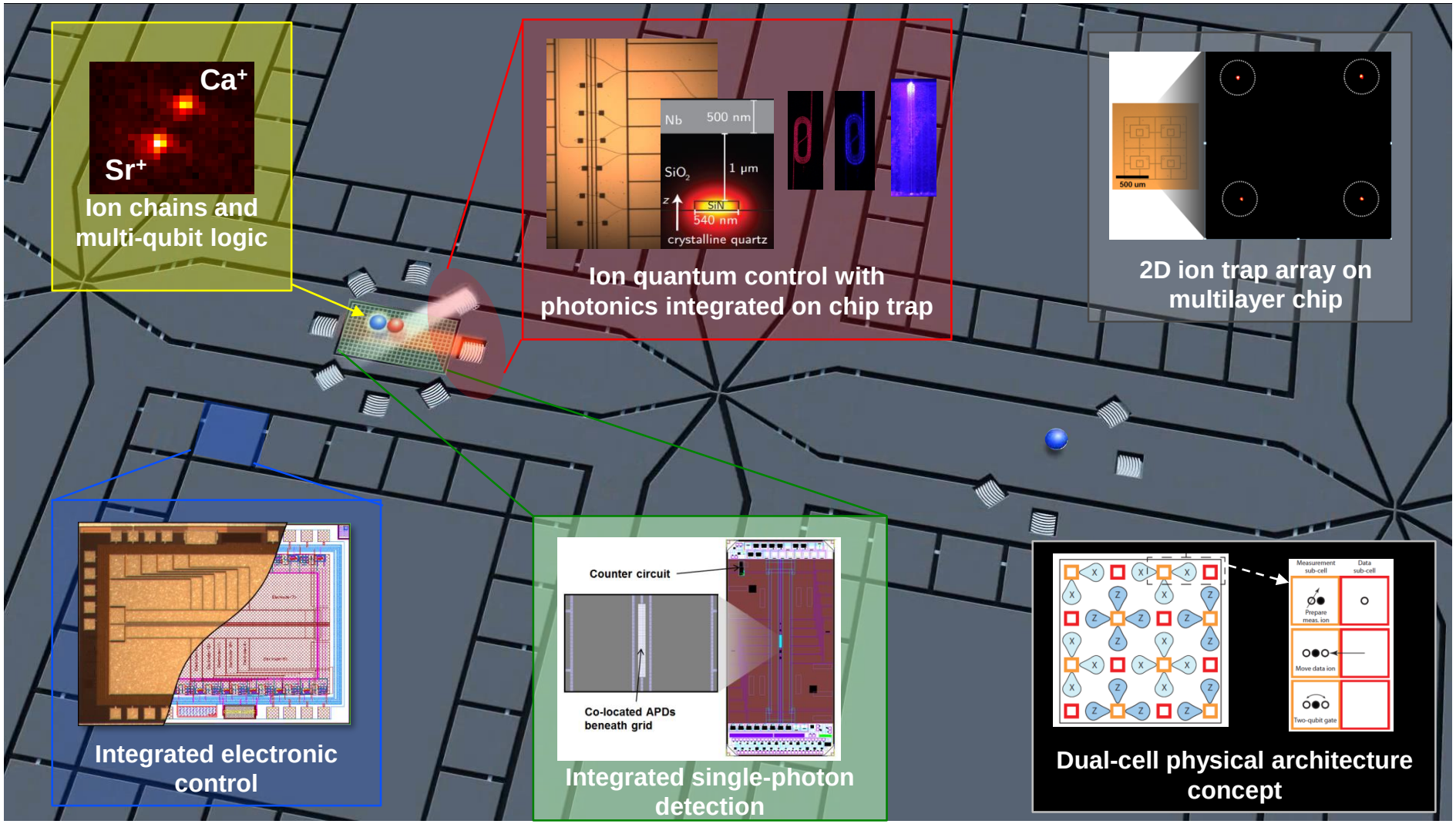
- **Integrated waveguides for light fan-out**
  - **Grating coupler optics direct light to ions**
- **Detection on-chip**
- **Tile cells in array for multi-qubit processing**
  - **Ions move to interact with neighbor ions**

Tiling Ion Cells



Trapped-Ion Array Critical Elements

Medium-Term Unit-Cell Integration



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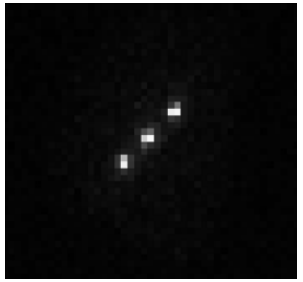
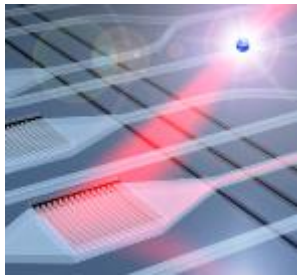
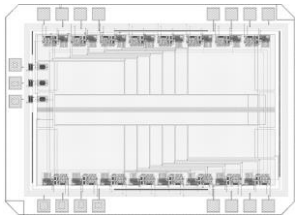
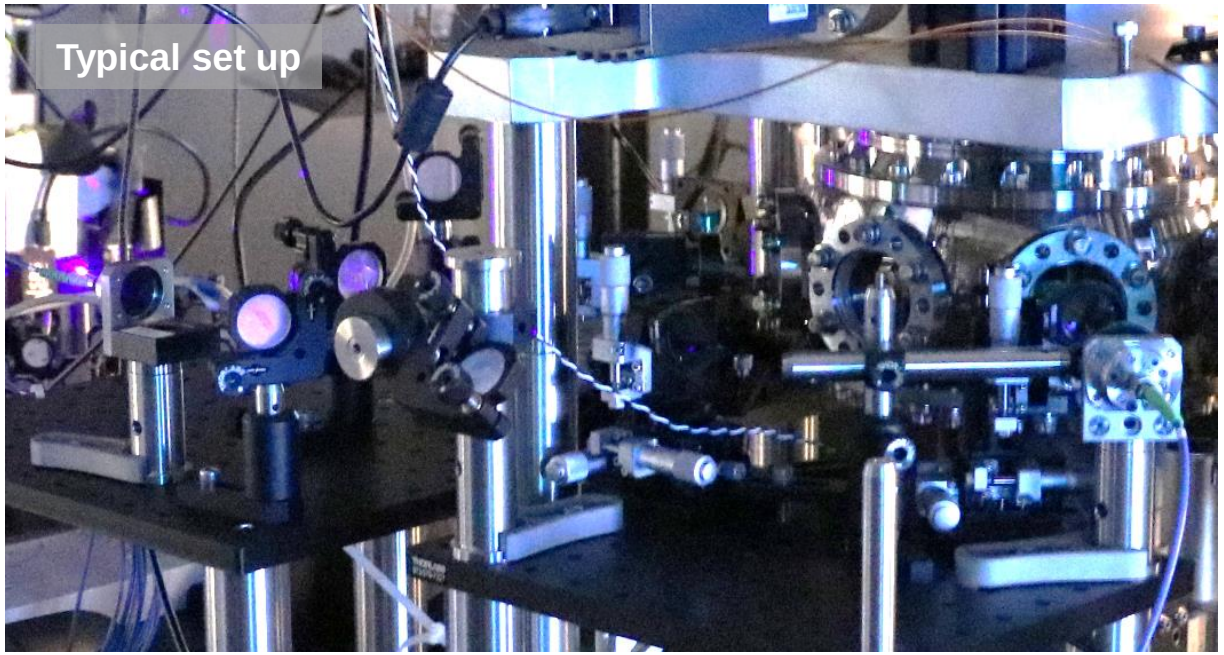


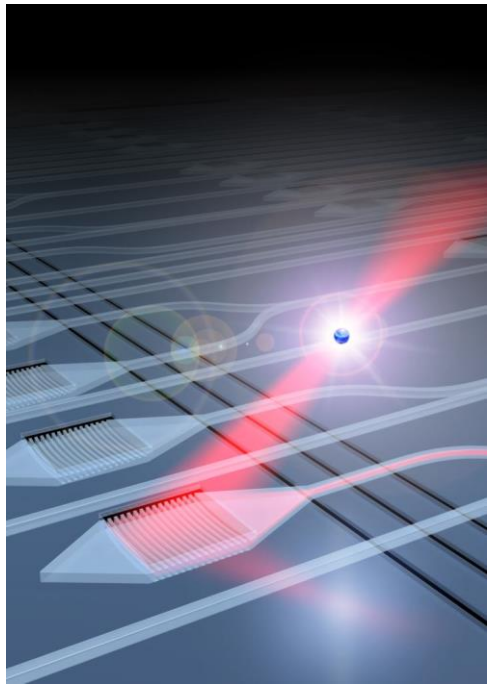




Reduced Beam-Pointing Instability



- Free space optics are supported outside the vacuum chamber far from the ion
  - Long lever arms
  - Subject to acoustic, thermal, and air-flow perturbations

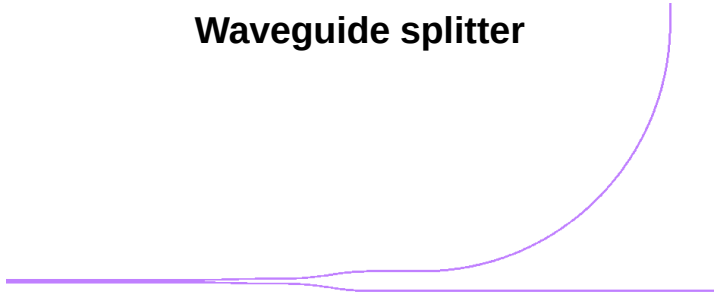


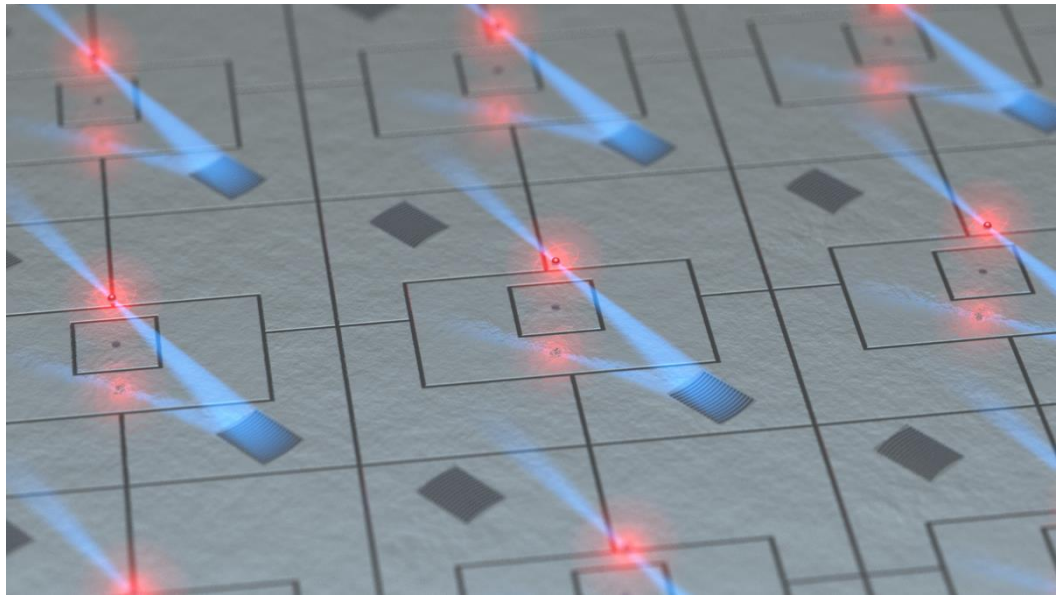
- Chip-integrated optics eliminate many of these shortcomings
  - Stable on-chip beam paths (can be fiber coupled to chip)
  - Final optic <100 um from ion
  - This last free-space path (grating-to-ion) is air-free

Addressing Arrays of Ions

- **Addressing many ion sites a challenge with free-space optics, particularly in 2D**
- **Chip-integrated beam paths reduce optics footprint**
- **On-chip splitters for fan-out**

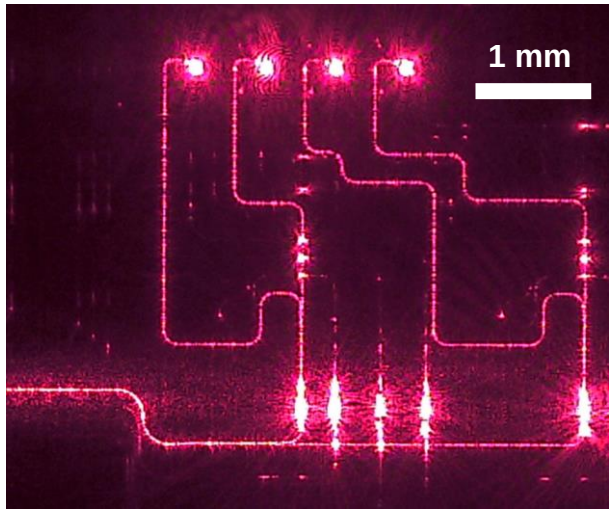
Waveguide splitter





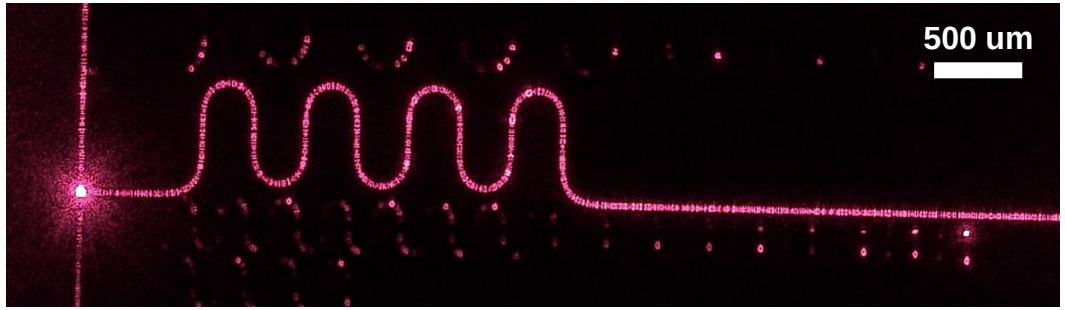
Array-clock concept

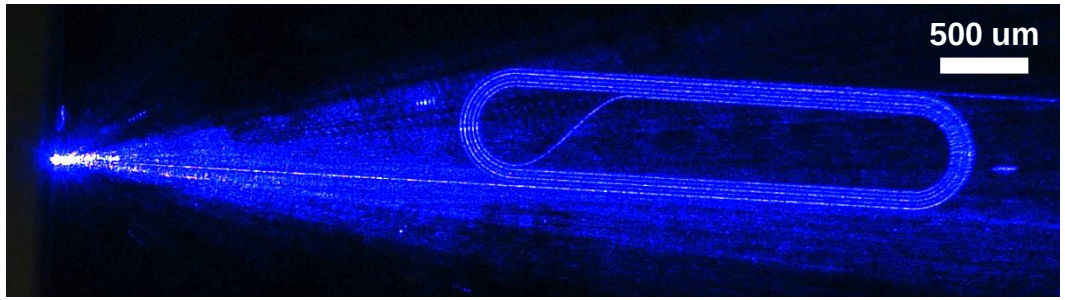
Microscope image of light in waveguides of 4-site array

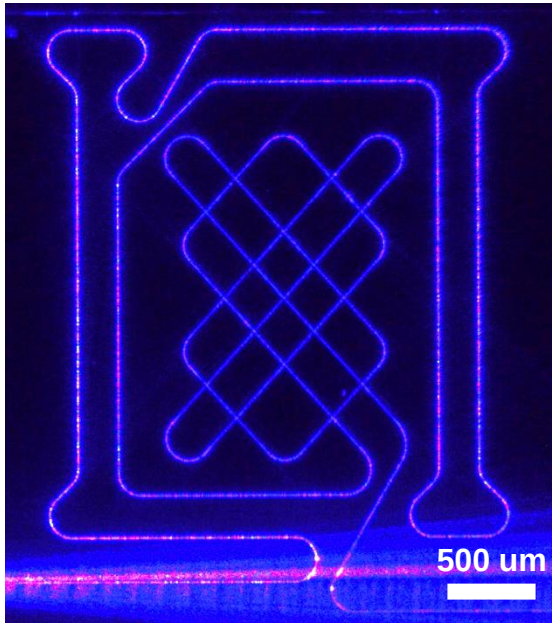


Single-Mode Waveguides

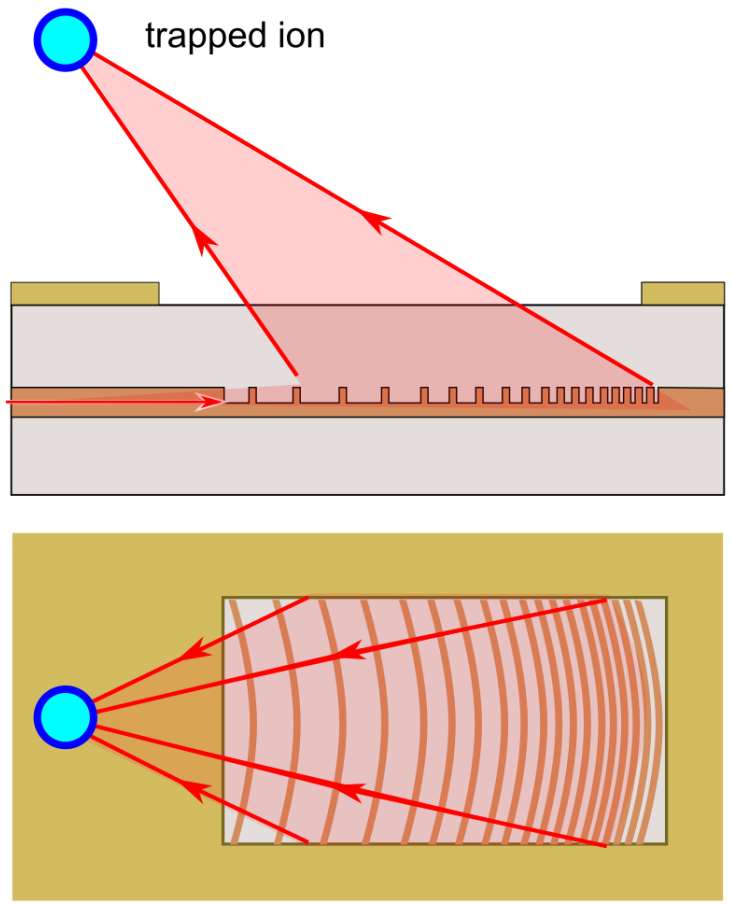
- **High-index core surrounded by low-index cladding**
  - **Typically sub-square micron MFD**
- **Like a fiber on a chip, but can be patterned with precise alignment to ion trap**
  - **Straightforward routing (bend radius depends on wavelength)**



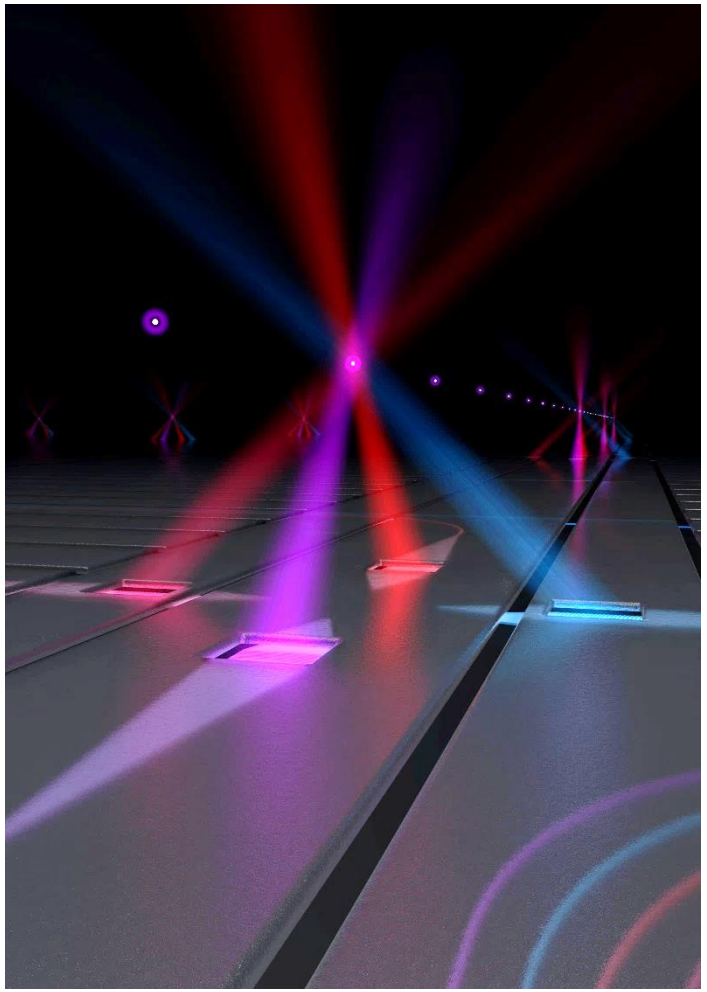




Grating-Based Waveguide-to-Beam Couplers



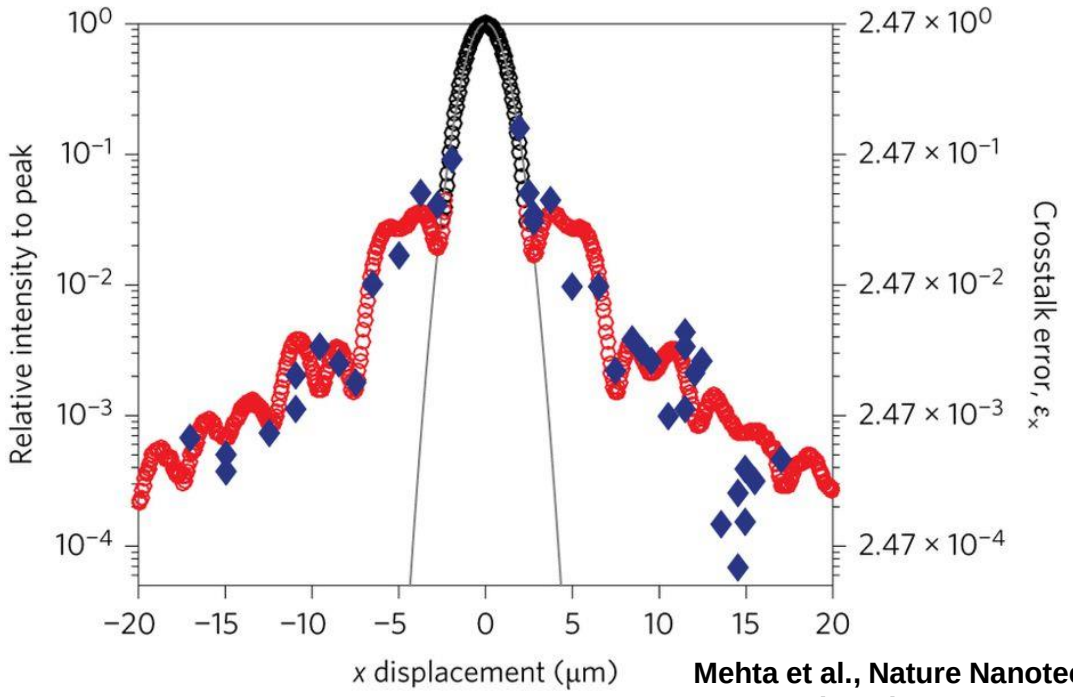
- At distal end of waveguide, periodically vary the index contrast
  - Can vary presence or depth of core material
  - Grating formed can diffract light into a beam
  - Emitted angle depends on period, wavelength, indices, etc.
  - Varying duty cycle and tooth curvature along waveguide can provide focusing
- Requires wavelength-scale feature definition



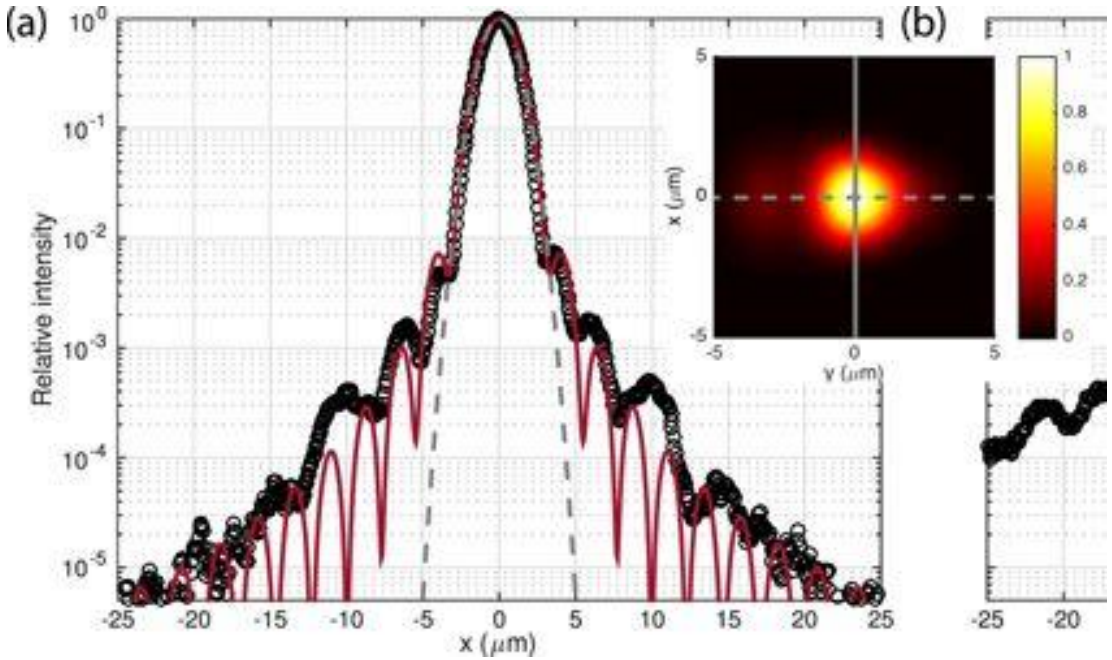
Dalgoutte and Wilkinson, Appl. Opt. 14, 2983 (1975)

Tightly Focused Beams

- **Reduced beam-pointing instability also reduces need to account for beam wandering**
  - **Beams can be smaller at ion locations; few-um diameter beam spots: grating-based optics**
  - **Higher useful intensity for given beam power**
  - **Potentially lower crosstalk**



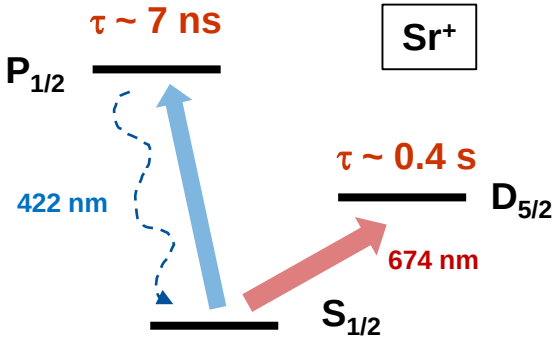
Mehta et al., Nature Nanotech. 11, 1066 (2016)

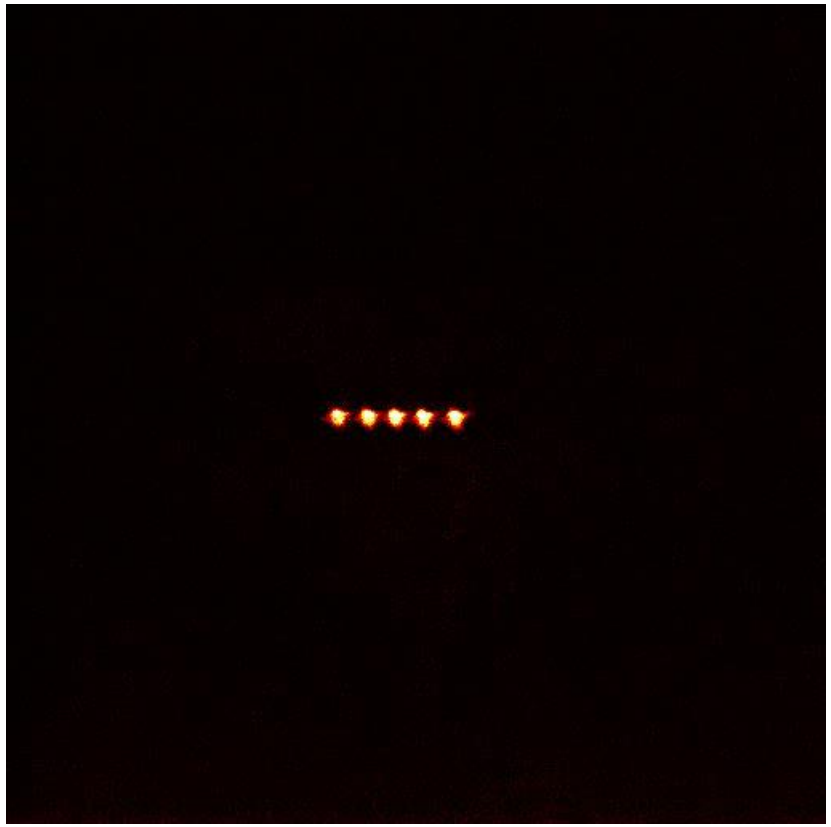


Mehta and Ram, Sci. Reports 7, 2019 (2017)

Individual Ion Addressing

- Grating coupled beam diam. 4 um along trap axis
  - Ion separation ~ 5 um
- Can address single ion in chain
- Movie: quantum jumps in center Sr^+ ion



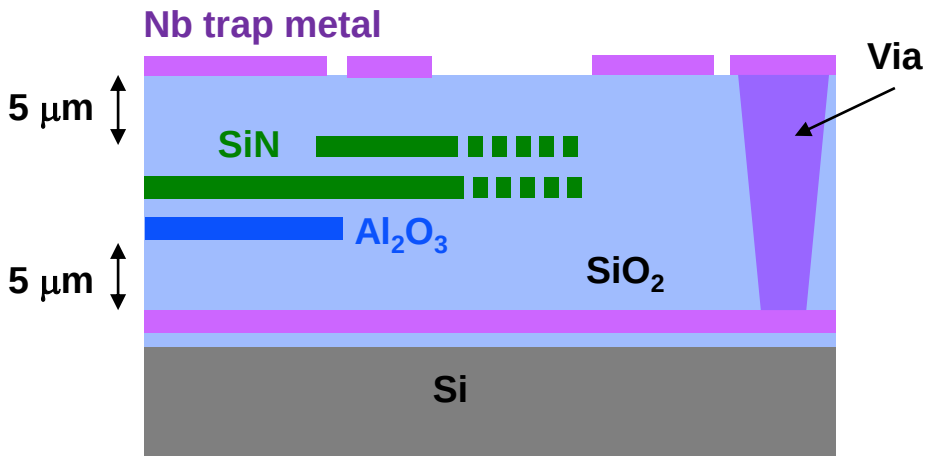


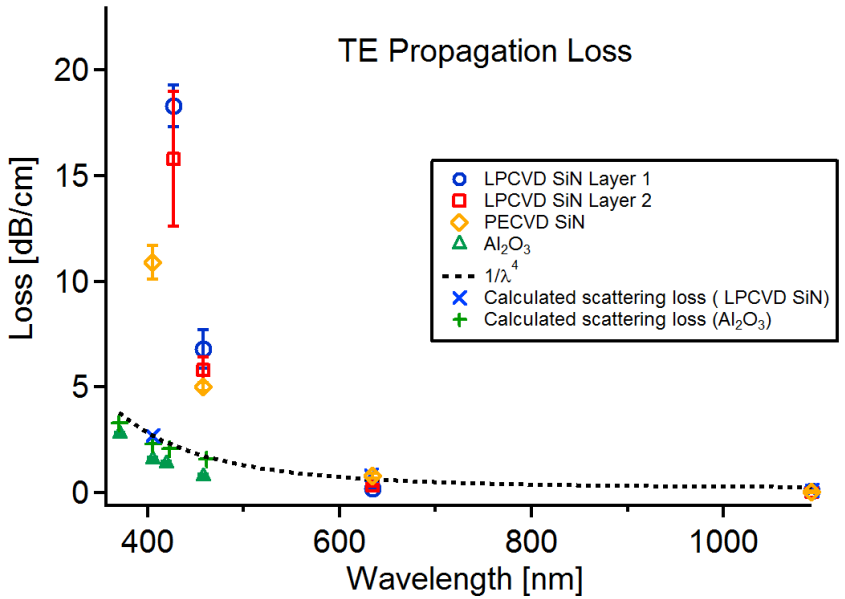
Diffraction-limited beam size from integrated optics

Mehta et al., Nature Nanotech. 11, 1066 (2016)

Integrated Photonics Multilayer Platform

- **Fabricated in LL's 8" wafer, 90-nm microelectronics laboratory**
  - **Low-loss, high-confinement routing**
    - **< 0.5 dB/cm from 600-1100 nm in SiN**
    - **< 3 dB/cm from 370-600 nm in Al2O3**
  - **Complete passive component library**
    - **High-efficiency grating couplers for all λ**
      - **60% grating efficiency demonstrated in red**
    - **Multi-layer alumina-to-SiN transitions**
    - **On chip tapers for fiber IO**
    - **Crossings, splitters, couplers**
  - **Metal layers beneath photonic elements**
    - **Allows for ground plane to provide electronic isolation from the silicon**





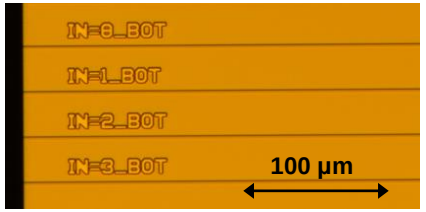
Sorace-Agaskar et al., IEEE JSTQE 25, 8201515 (2019)

West et al., APL Photonics 4, 026101 (2019)

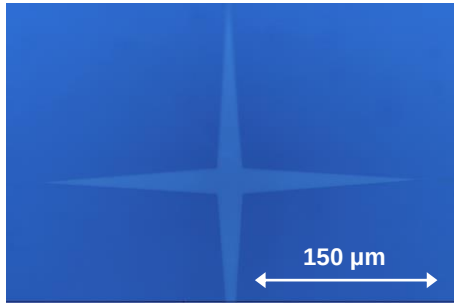
Visible Light Platform Development (SiN, Al_2O_3)

Selected Components

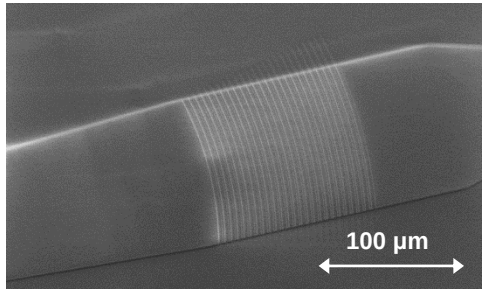
Input-Output Couplers



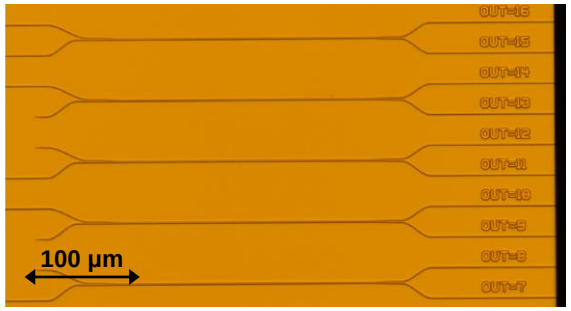
Crossings



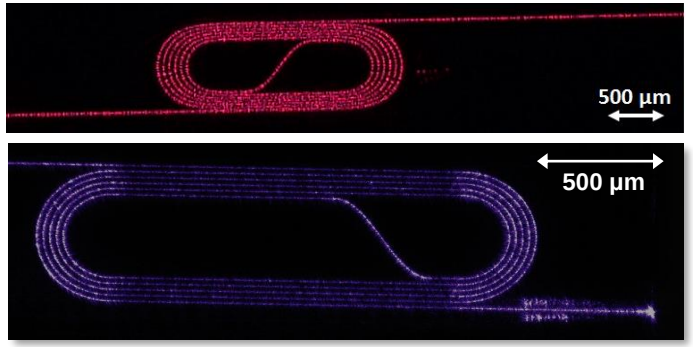
Focusing Grating Couplers



Splitters



Waveguides

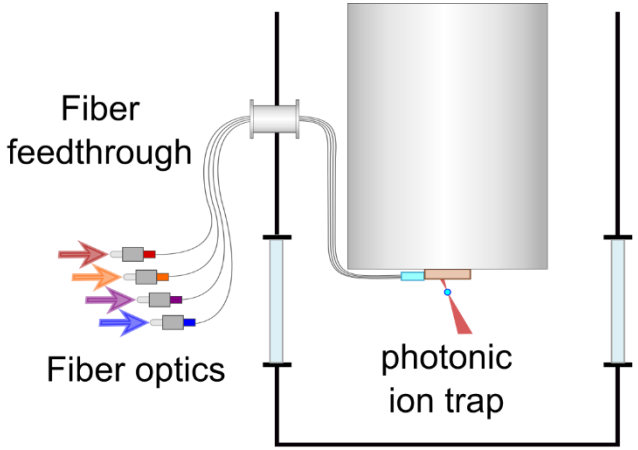


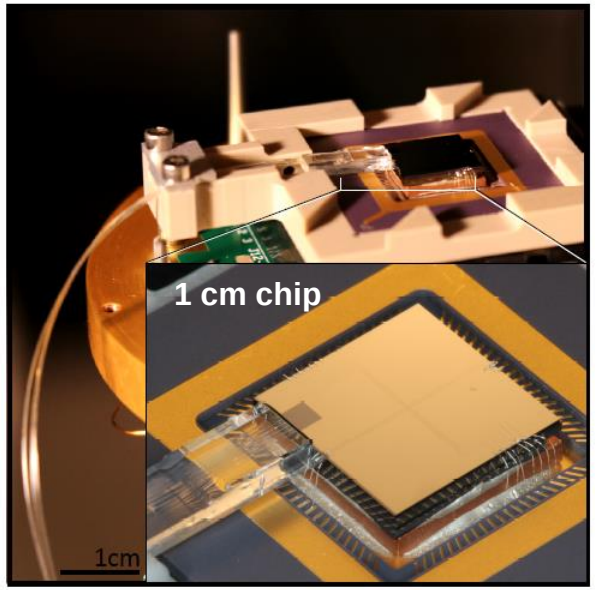
C. Sorace-Agaskar *et al.*, *IEEE JSTQE*, 2019

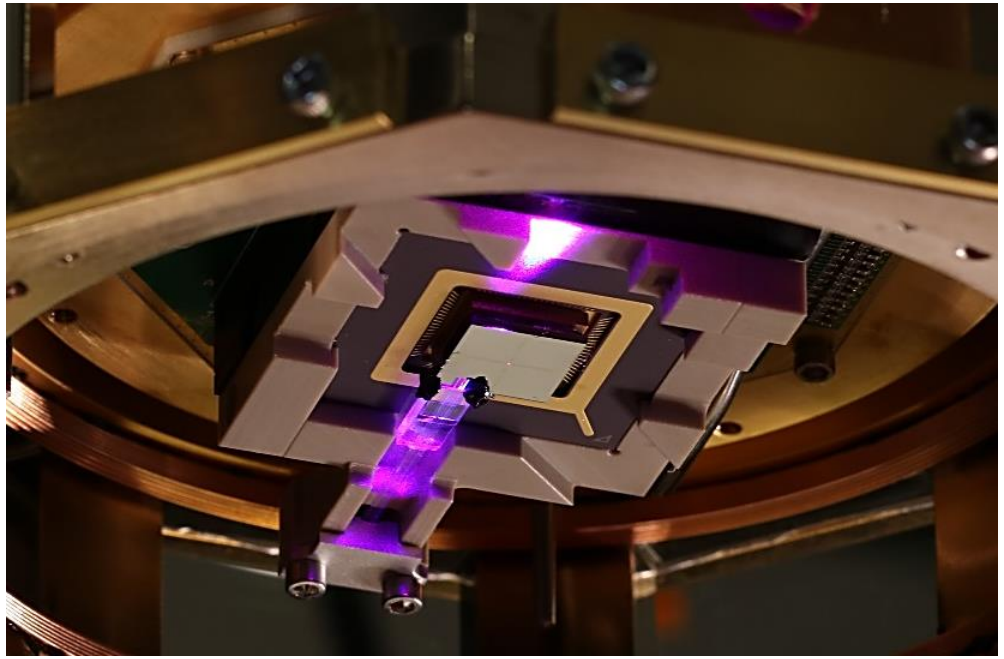
Platform information:

- Designs cover 370 - 1092 nm (Yb+, Sr+, Ca+)
  - ~10 fundamental devices at 14 distinct wavelengths
- Performance:
  - SiN Loss < 0.3 dB/cm (Yellow to NIR)
  - Al_2O_3 Loss 1-3 dB/cm (NUV to Green)
- Supports multiple photonic layers and metallic trap layers

Fiber Attach and Installation in Cryogenic UHV System

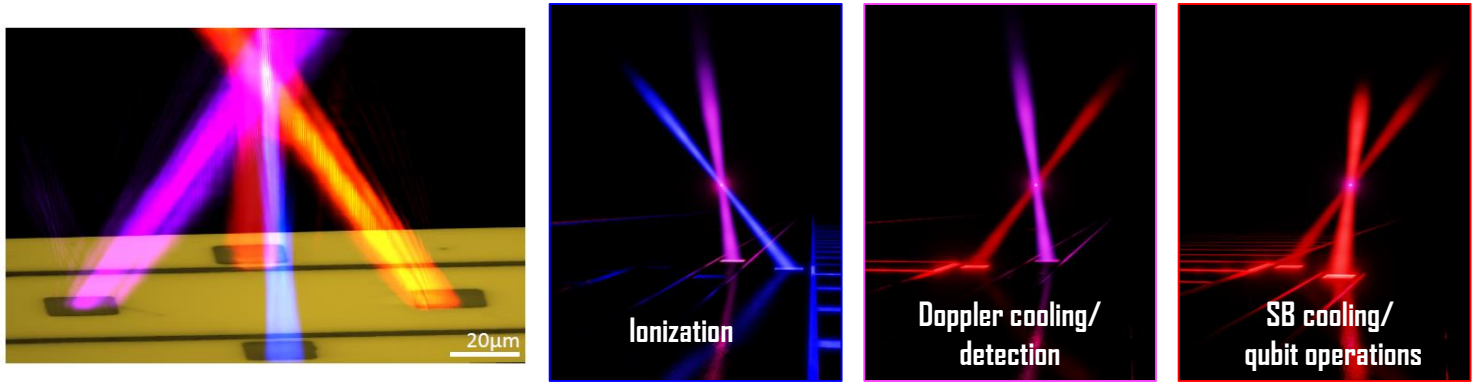


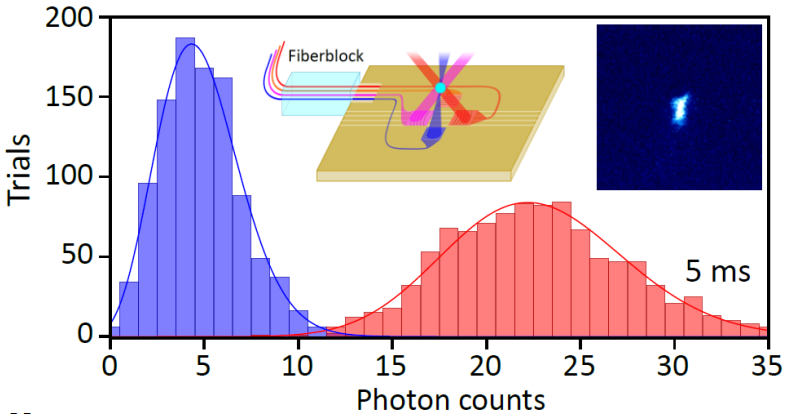


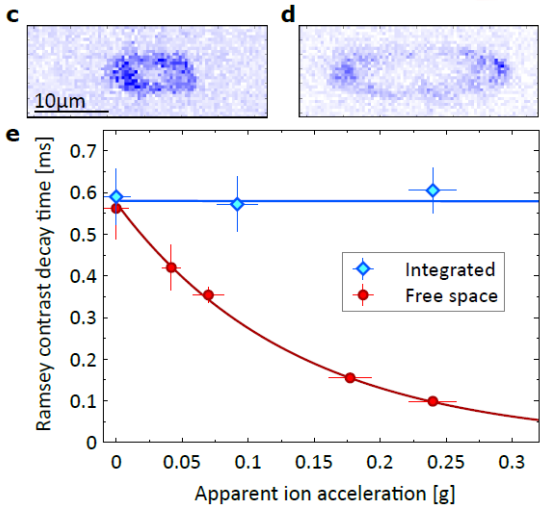


Multi-Wavelength Integrated Optics

- **Operations on Sr^+**
  - **461/405 nm photo ionization**
  - **422 nm cooling/detection**
  - **1092 nm repump**
  - **674 nm sideband cooling, coherent operations**
  - **1033 nm qubit quenching**
- **Verified ex-situ beam profiles in-situ with ion**
- **Photonic illuminated detection**
  - **99% detection fidelity using integrated delivery of light**
- **Vibration-resilient qubit coherence**
  - **Common-mode platform vibration**



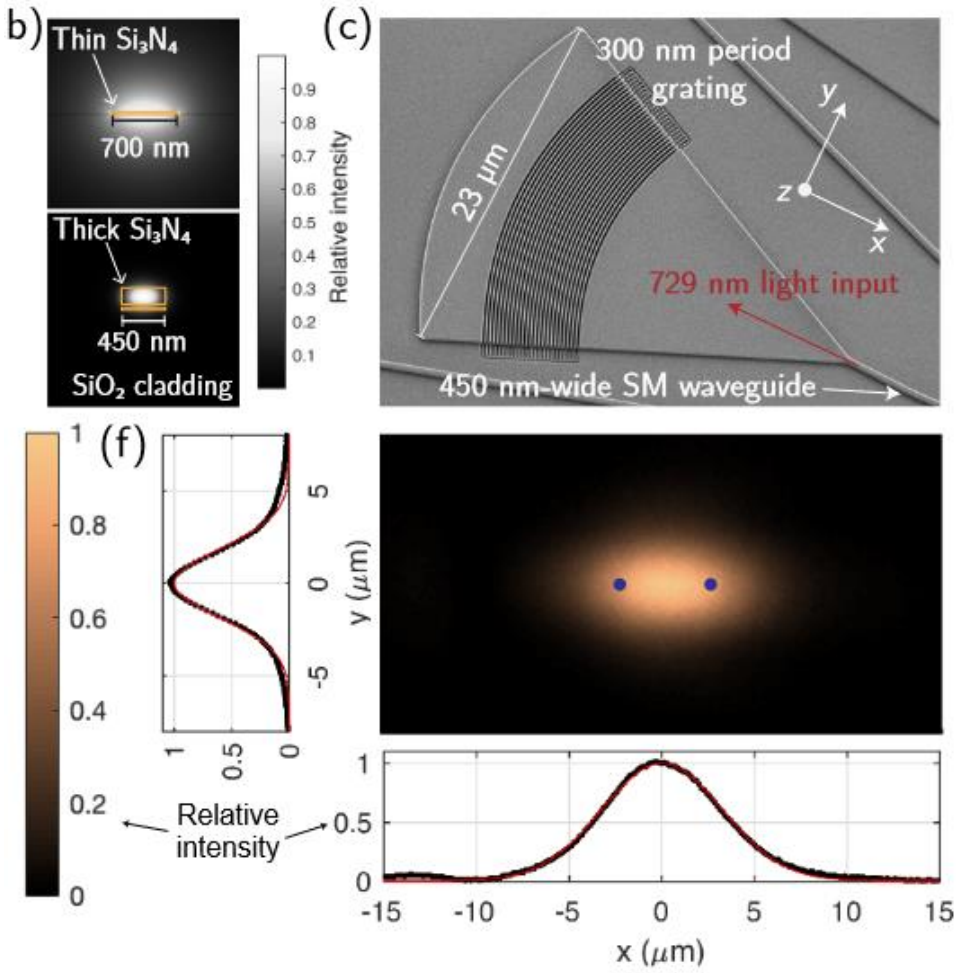




Niffenegger et al., Nature 586, 538 (2020)

Multi-Qubit Gates with Integrated Photonics

- **ETH Zurich: complementary work**
  - **Single wavelength integrated in chip for Ca^+ logic (729nm)**
  - **High-fidelity two-qubit gates (F ~ 99.3%)**
  - **Good on chip coupling (~2 dB loss) using multi-layer edge-coupler**
- **With multi-wavelength capabilities, provides a platform with significant potential**
  - **Need to address potential trade offs**
  - **Scatter, low input coupling, power handling**

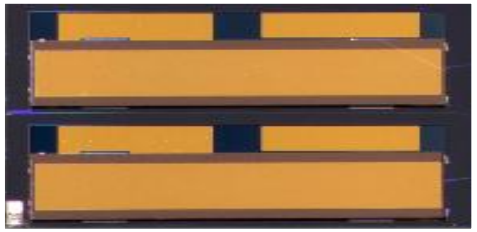


Mehta et al., Nature, 586, 533 (2020)

Expanded Silicon Nitride Platform

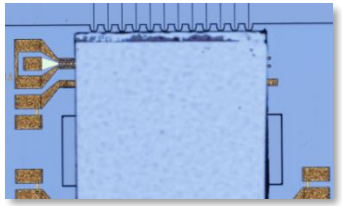
Pick-and-Place Component Integration

InP Laser



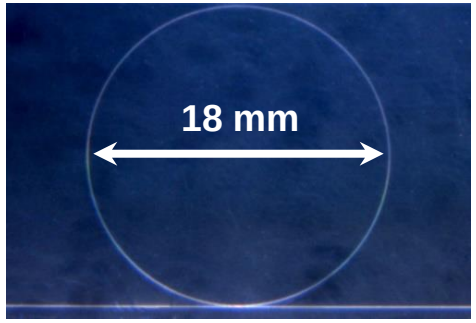
- 312 mW single mode laser output on-chip

High-Speed InP Photodiode Array

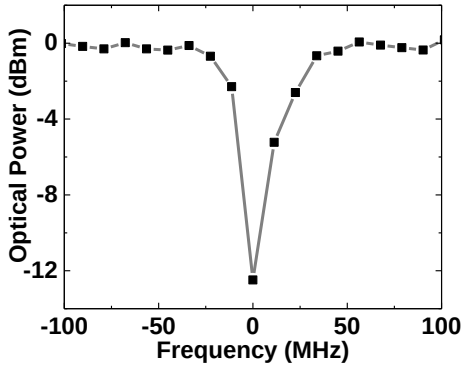


- Current: 45 GHz, 0.05 A/W
- Future: 80 GHz, 0.2 A/W

Ultra-Low-Loss, Low-Confinement SiN

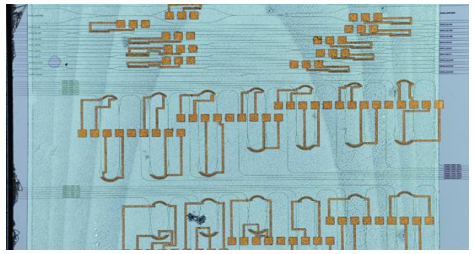


- 0.5 dB/m Loss



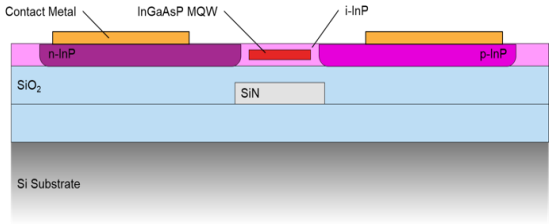
Bonded Thin-Film Materials

LiNbO2 (Modulators)



- Passive loss 0.4 dB/cm
- Preliminary demonstration of modulation

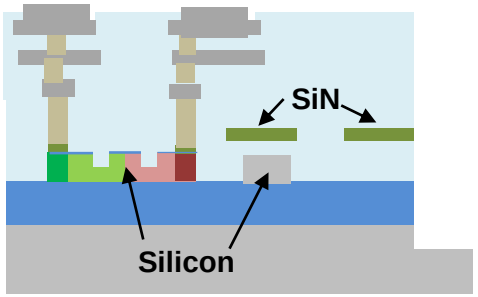
III-V Films



- Individual fabrication steps successfully demonstrated
- 90% bonding yield

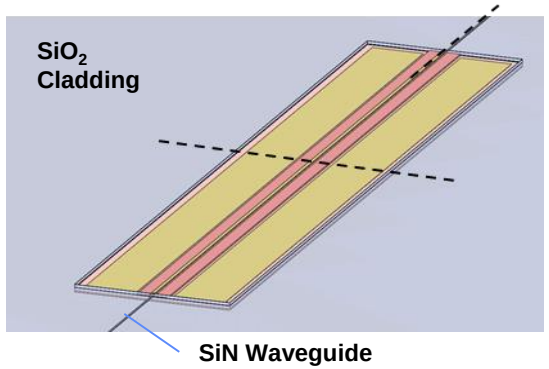
Monolithic Integration

Silicon Photonics



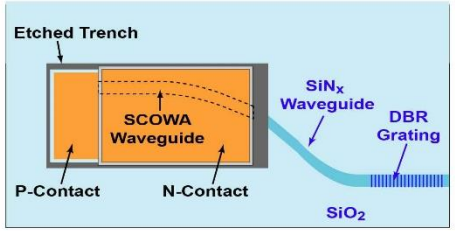
- Low loss preserved with integration

Heteroepitaxial III-V Growth

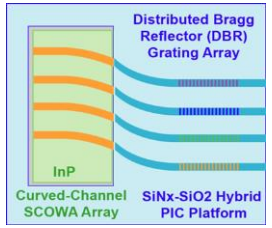


Photonic Multi-Chip Module

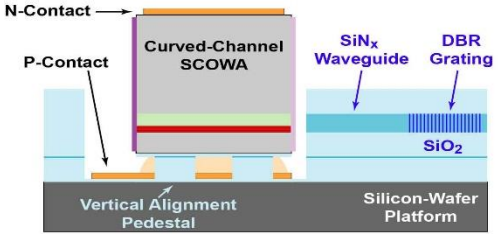
TOP VIEW



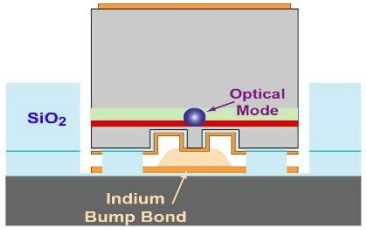
4 Element Array



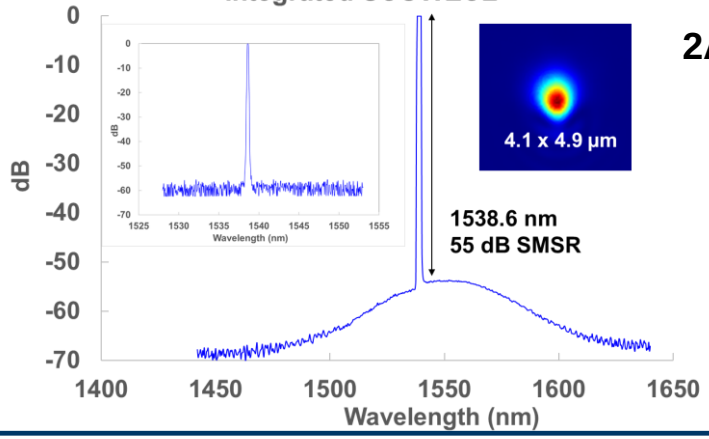
LONGITUDINAL CROSS-SECTION



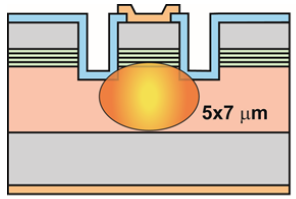
TRANSVERSE CROSS-SECTION



Normalized Optical Spectrum for a Hybrid Integrated SCOWECL

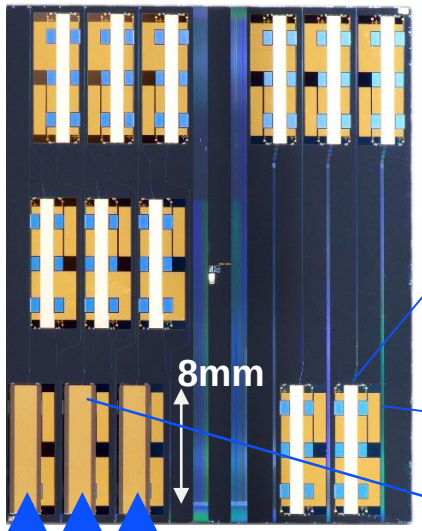


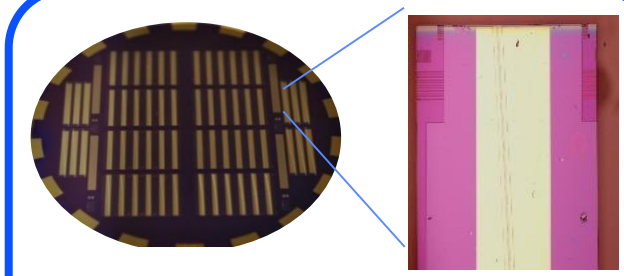
312 mW at 2A SCOWA bias



PIC Hybridization Submount

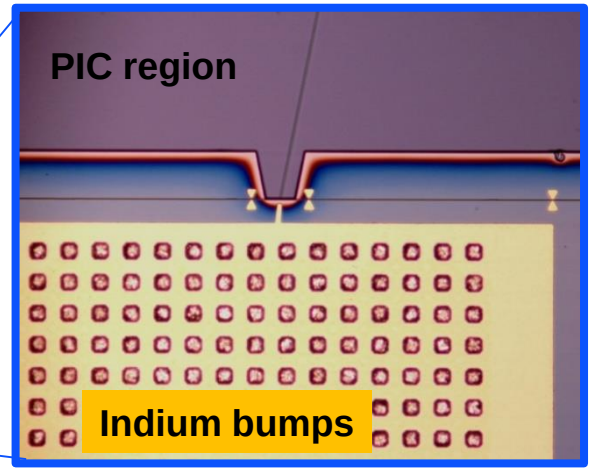
14 Insert Slots



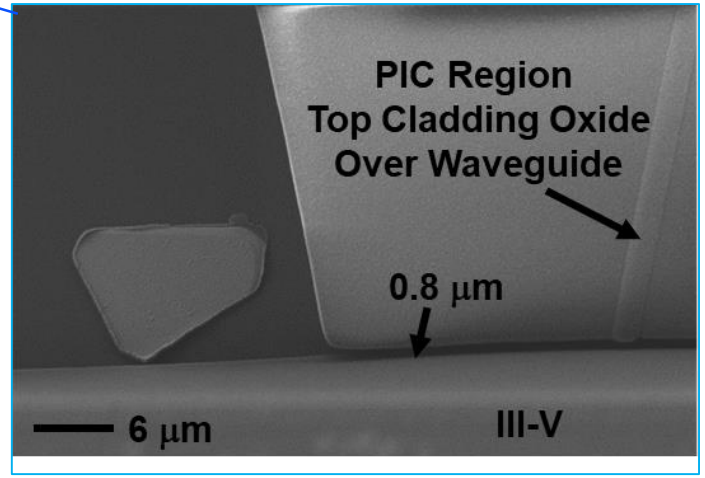


InP SCOWA Insert Devices

Silicon Nitride PIC on Silicon



Input Facet with III-V SCOWA



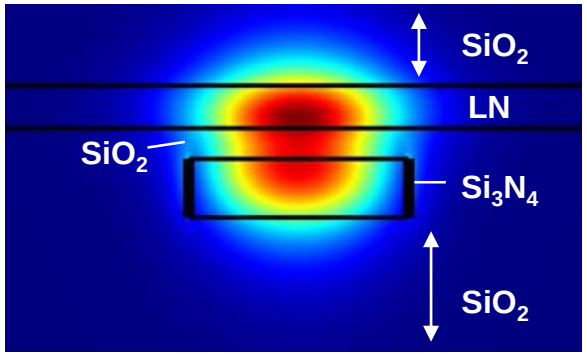
D. Kharas et al. IEEE Phot. J. 12, 1504612 (2020)

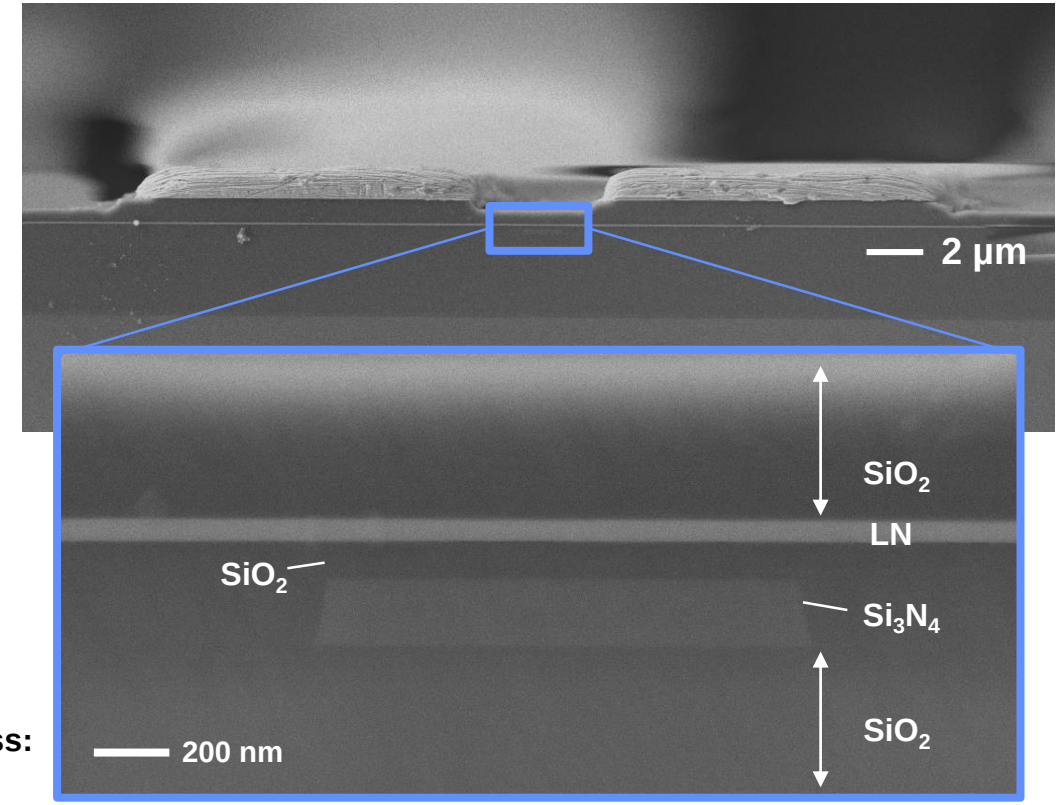
SCOWA: Slab-coupled optical waveguide amplifier
SCOWECL: Slab-coupled optical waveguide external-cavity laser
SMSR: Side-mode suppression ratio

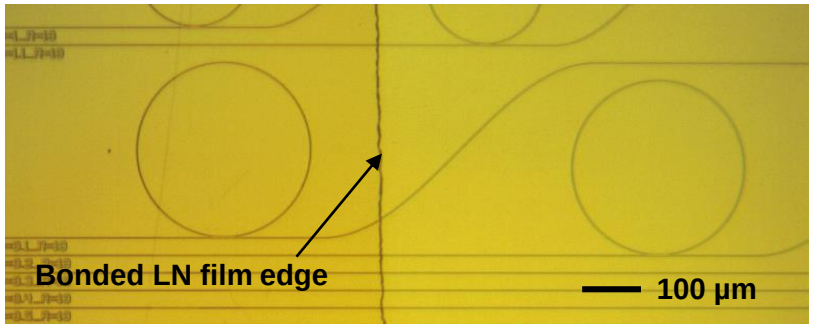
Thin-Film Lithium Niobate Integrated with SiN PICs

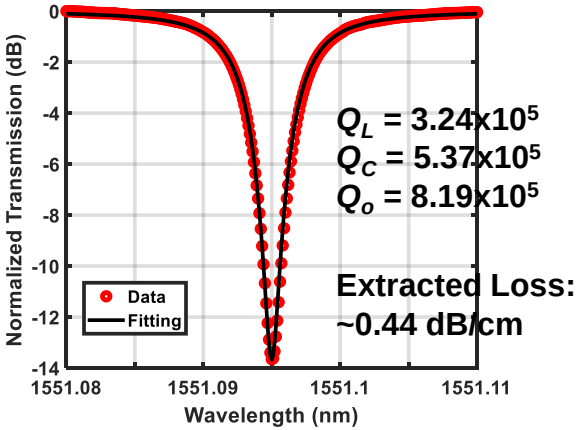
Heterogeneous $LiNbO_3$-Si_3N_4 waveguide

TE fundamental mode
λ = 1550 nm
n_{eff} = 1.6644
n_g = 1.9242









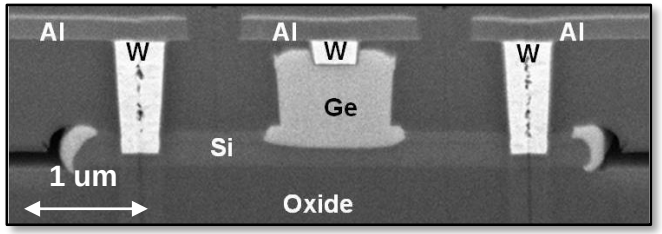
Al_2O_3 based ALD bond demonstrates one of the lowest measured losses in LN-SiN ring resonators

S. Ghosh, S. Yegnanarayan (MIT-LL)
LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Silicon Photonics Platform Module

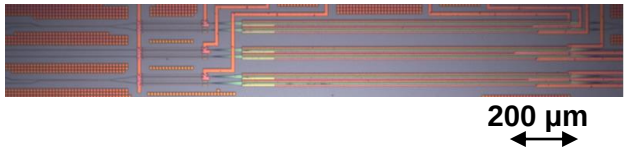
Selected Components

Germanium Photodetectors



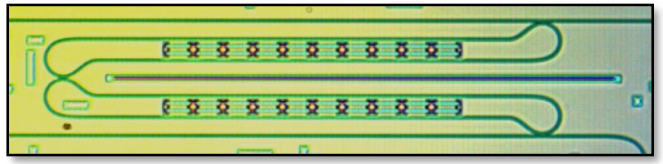
Responsivity = 0.8 A/W,
Dark current = 6 nA
BW > 15 GHz

High-Speed Modulators



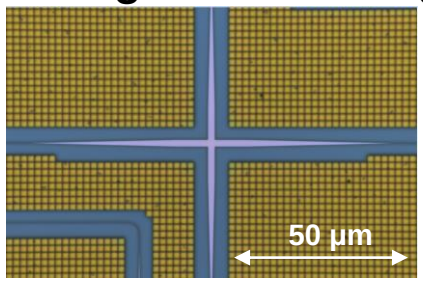
$V_{\pi}L$ = 1 V-cm
BW > 15 GHz

Narrow Band Optical Filters



Loss <<1 dB
Extinction >20 dB
BW ~ 1.2 GHz

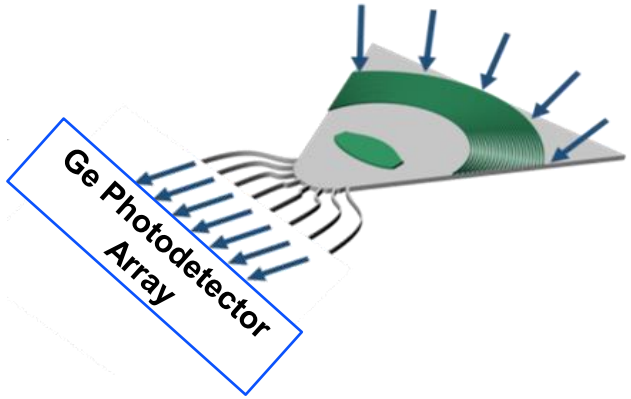
Waveguide Crossings



Loss < 0.05 dB
Cross-talk < -50 dB

- And many others…

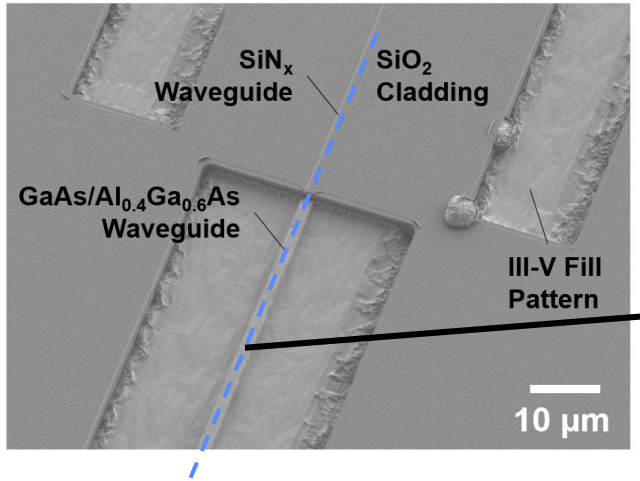
- **Process information:**
  - Good performance, waveguide loss ~ 1 dB
  - New Ge reactor will allow for trusted processes
  - Cadence based process design kit
  - Preliminary work on integration with CMOS, III-Vs, and SiN
    - No increase in loss with Si-SiN integration



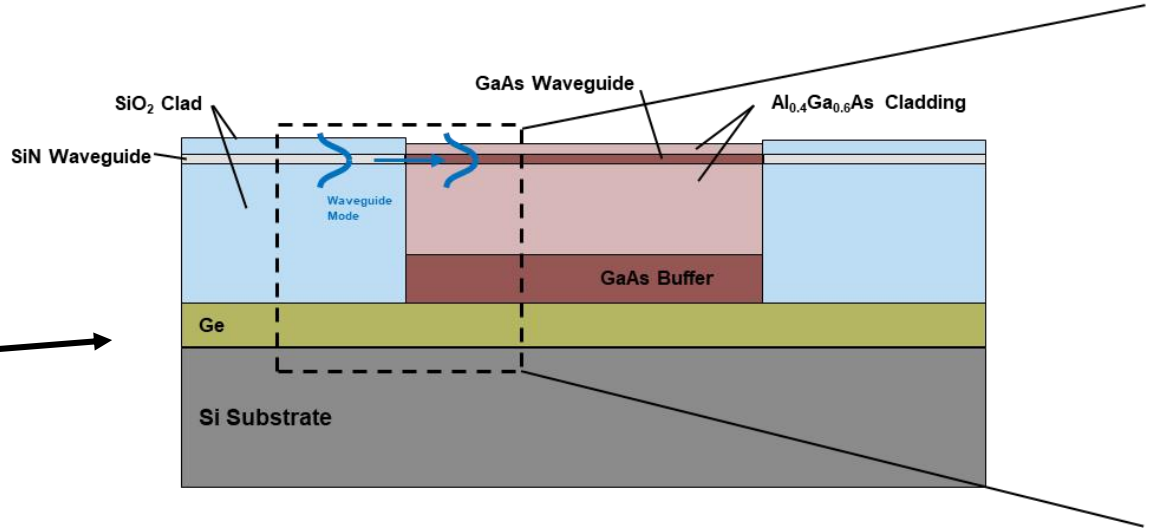
C. Sorace-Agaskar et al. (MIT-LL)

Heteroepitaxial III-V/SiN Integrated Photonics (HIP)

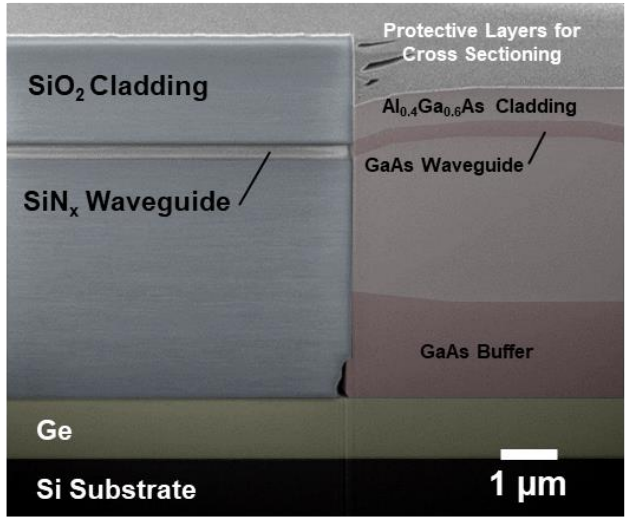
Angled-View SEM of III-V/SiN Hybrid Photonic Integrated Circuit



HIP Longitudinal Cross-Section



Cross-Section SEM
(False Color)

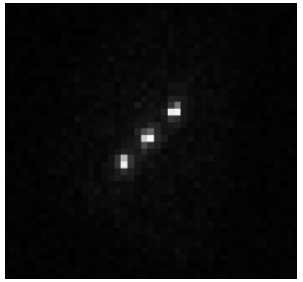


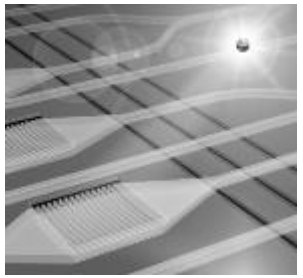
- **Objective: Realize SiN waveguide-coupled III-V devices (e.g., modulators, photodiodes, opt. amplifiers)**
- **Status:**
  - **Demonstrated growth of GaAs/AlGaAs on silicon substrates with flush interface to SiO_2 facets**
  - **Threading dislocation density of 4×10^6 cm^{-2} for GaAs/AlGaAs heterostructures grown selectively on Si, sufficient for high-performance optoelectronic devices**
  - **Demonstrated efficient optical coupling between heteroepitaxial III-V and SiN waveguides**

Heidelberger, Sorace-Agaskar (MIT-LL); Lee (UIUC)

Outline

- Platforms for quantum information processing
- Trapped-ion quantum computing and sensing
  - Concept for trap array with integrated controls
- Integrated Photonics Development
  - Visible platform: Al_2O_3/PECVD SiN (low loss, multi-layer, CMOS-compatible)
  - Ion operations with multiple wavelengths of light, on-chip
  - Expanded photonics platform: potential for enhanced QIP functionality
- **Integrated Electronics**
  - **Monolithic integration of electronic controls for trapped ions**
  - **Photon detection and 3D integration**
- Near-Term Collaborations Utilizing the Ion Platform

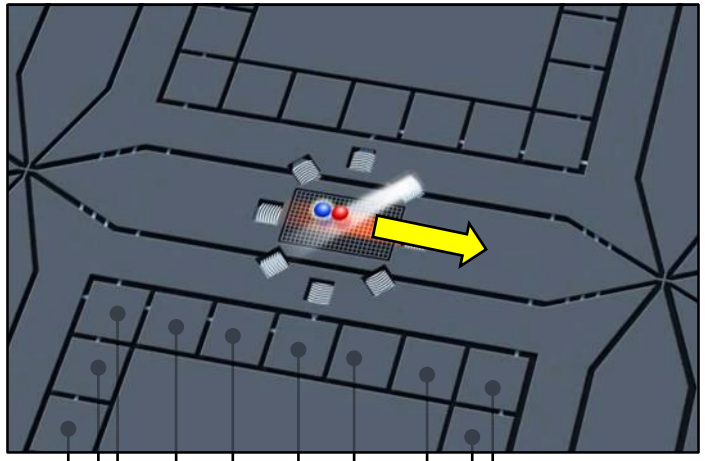




Integrated Electrode Control

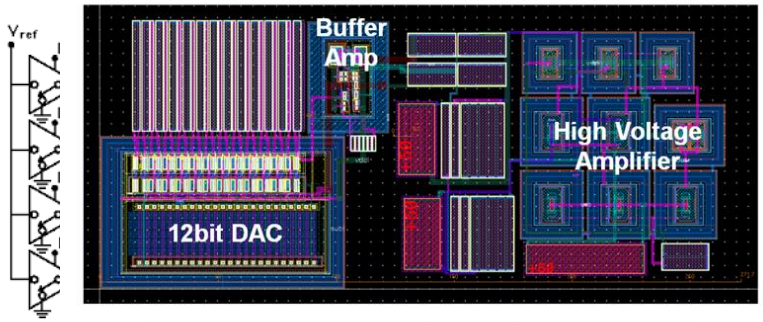
Development of integrated control to enable ion movement for high connectivity and potential control

- **Ion movement brought about by dynamically varying electrode voltages (+/-8 V range)**
- **DACs integrated in CMOS**
  - **Low voltage CMOS for DAC**
    - **Compact, best technology nodes**
  - **High voltage CMOS amplifier**
    - **Larger, physically buffered circuits**
- **In-house design; foundry fabrication for proof-of-principle demos**



$V_1(t)$ … $V_i(t)$ … $V_N(t)$

~ 250 µm

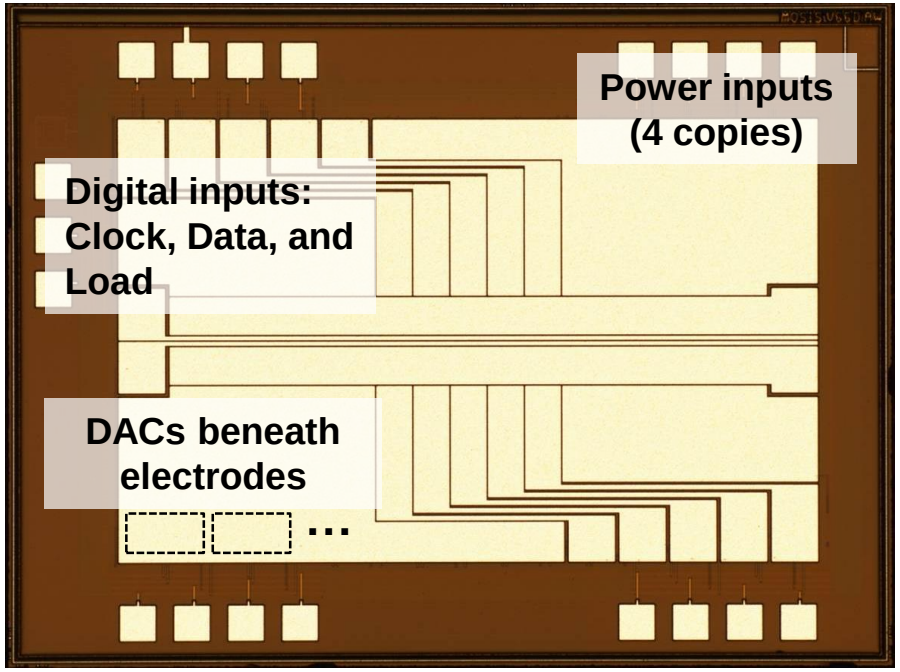


Layout of control block for single DC electrode

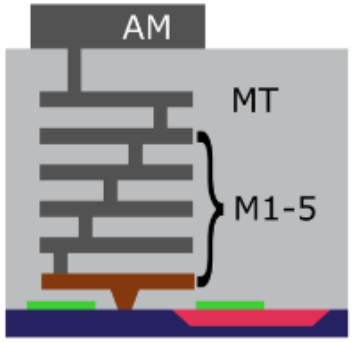
LV CMO

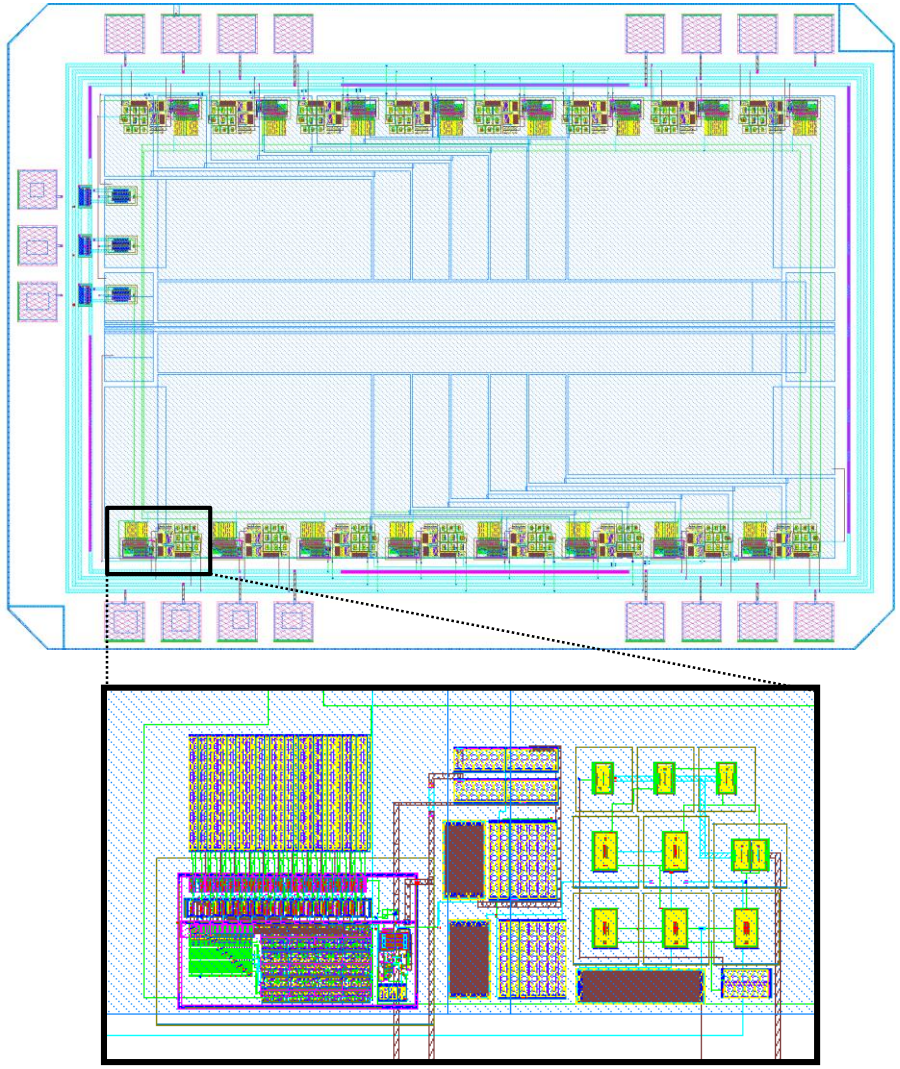
DAC: Digital-to-analog converter

DACs Integrated with Ion Trap



Layer Stack

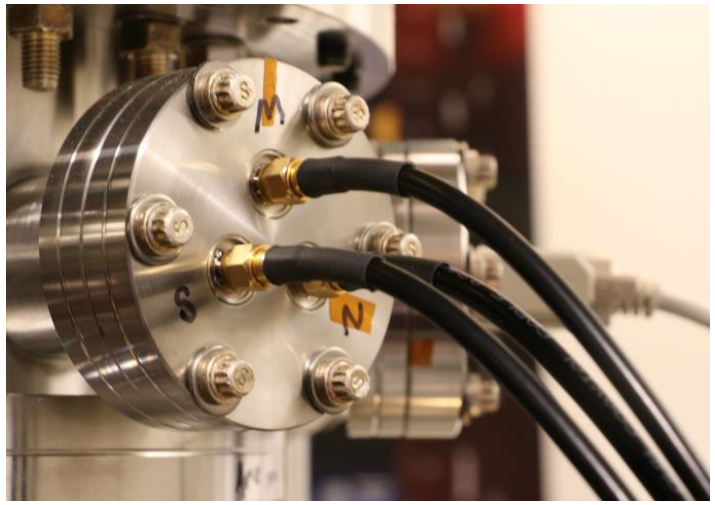


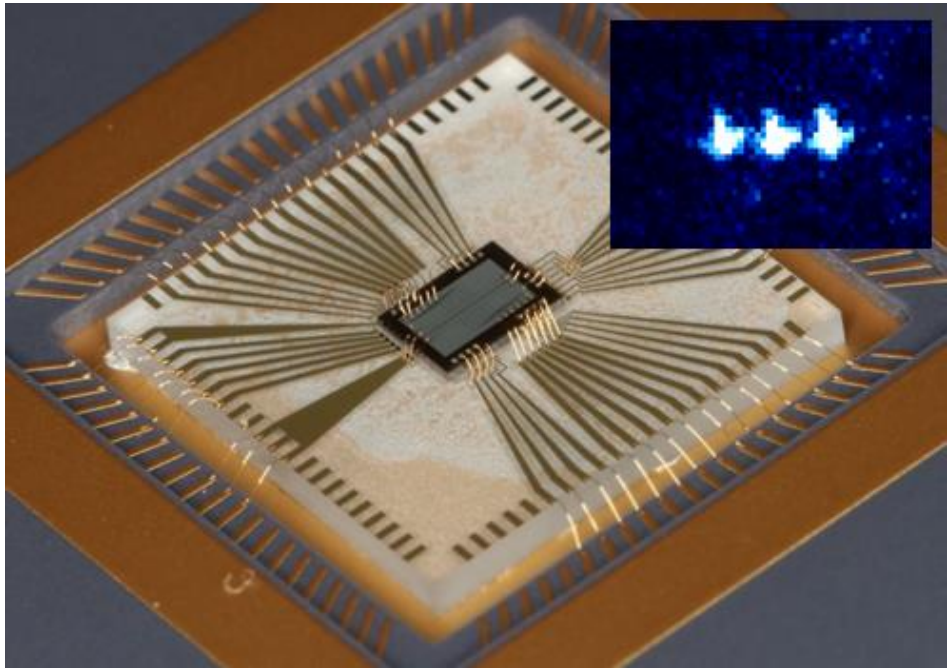


- **Linear surface-electrode trap chip (~2mm x 3mm) with 16 DACs integrated under trap electrodes**
  - **Inputs are for SPI bus and for power (V_{dd}, V_{ss}, etc.)**
- **Only serial digital inputs need updating to transport ions**

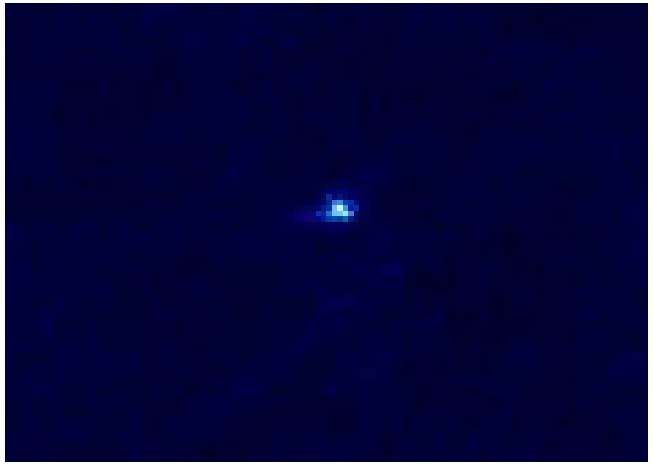
Ion Motion Using On-Chip Electronics

Three serial lines control 16 electrodes





Movie: Ion movement using integrated DAC control



Demonstrated trapping and moving of ions using integrated electronics

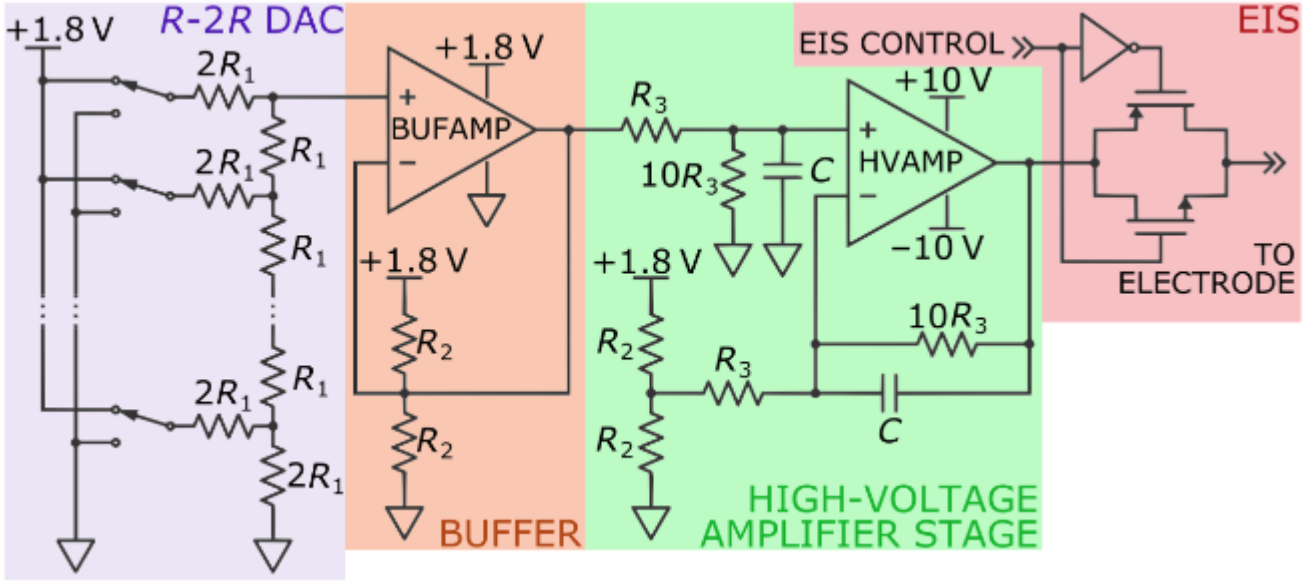
Stuart et al., Phys. Rev. Applied 11, 024010 (2019)

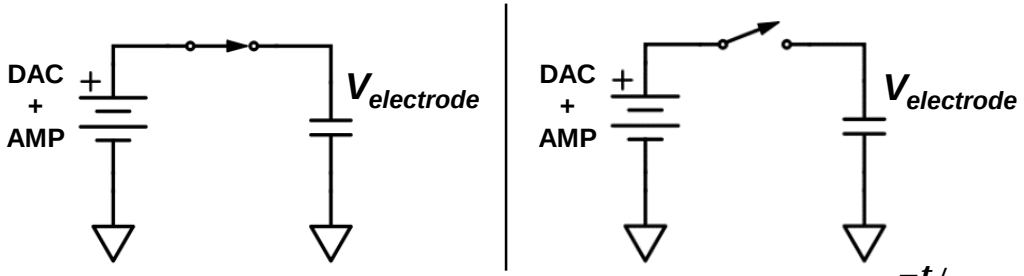
Switchable Filtering

- **Average motional state of the ion, $\bar{n}$, is directly sensitive to voltage noise on trap electrodes**

$$\dot{\bar{n}} = \frac{q^2}{4m\hbar\omega_t}\frac{S_V(\omega_t)}{D_{eff}^2}$$

- **Idea: use an analog switch between the amplifiers and the electrodes to isolate the ion from voltage noise**
  - **Electrode-isolation switch (EIS)**
  - **Since electrode is primarily a capacitive load, voltage will be maintained for reasonable times**
  - **Electronic noise can be greatly reduced in this configuration**

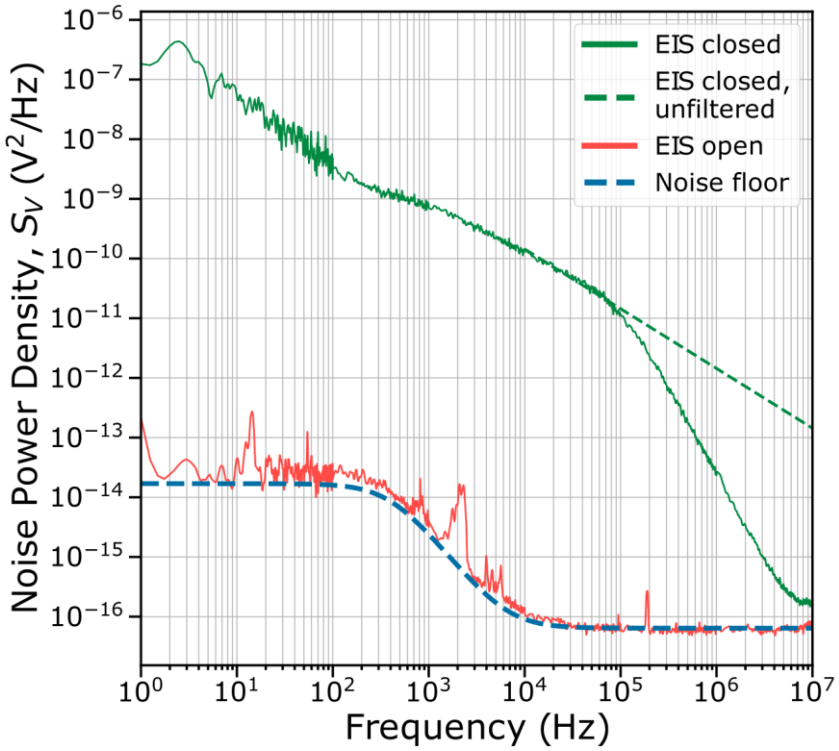


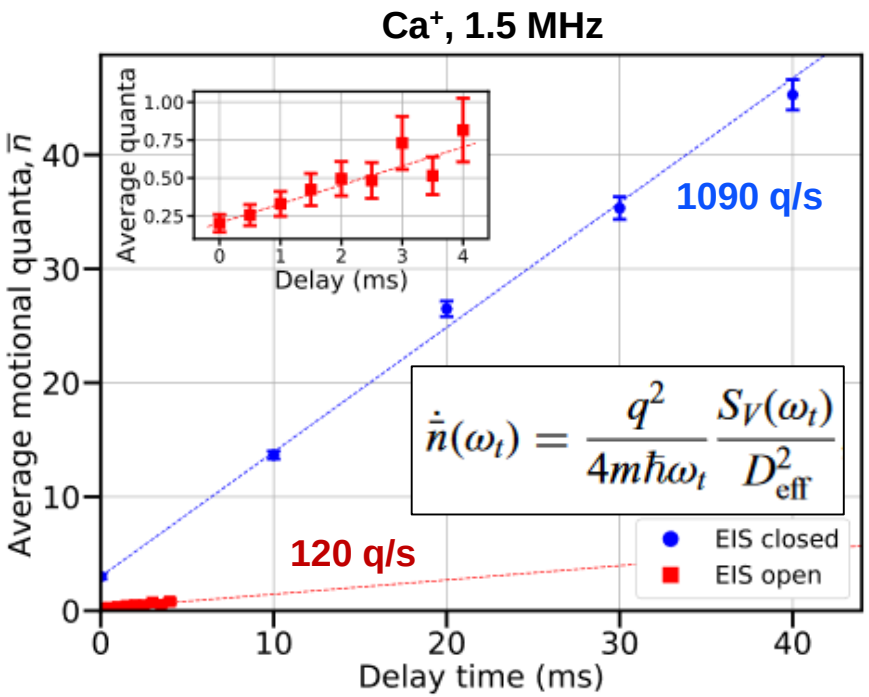


$$V_{electrode} = V_{DAC} + V_{noise} \qquad V_{electrode} = V_{DAC}\, e^{-t/\tau}$$

Stuart et al., Phys. Rev. Applied 11, 024010 (2019)

Dynamic Electronic-Noise Filtering



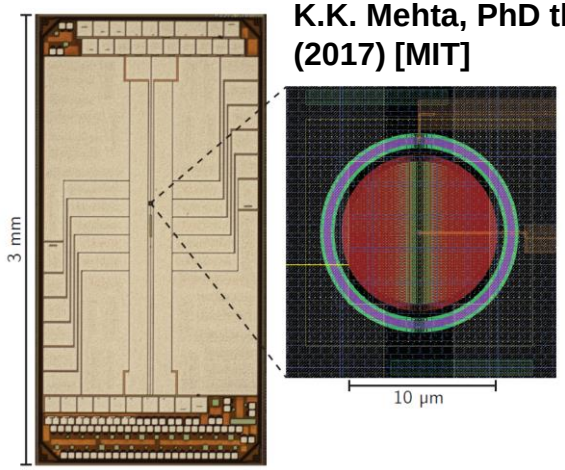


- **Electrode-isolation switch (EIS) on each channel uses FETs to create large open-state resistance between DAC and electrode**
  - **Measured noise spectrum of DACs on bench**
  - **Verified level by measuring ion heating rate (proxy for electric-field noise)**
  - **Heating consistent with direct measurement (for ~50K chip temperature)**

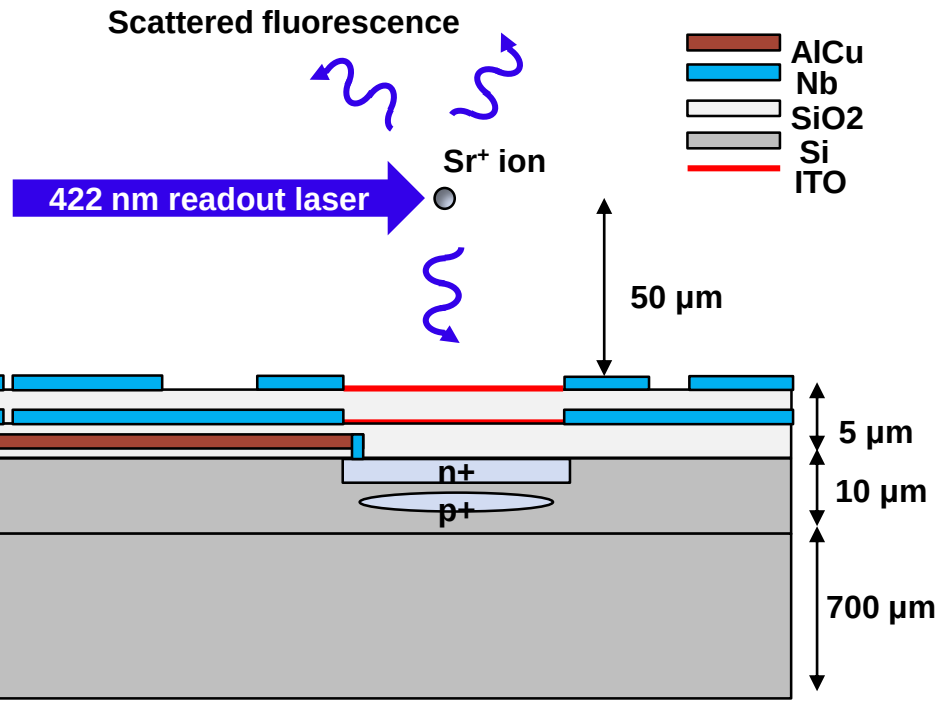
Stuart et al., Phys. Rev. Applied 11, 024010 (2019)

Avalanche Photodiodes for Readout

- **On-chip Geiger-mode avalanche photodiodes (APDs) for ion state readout**
  - **Replace external high-NA lens and photomultiplier tube (optics free)**
- **Trap-integrated APDs tested on the bench (room temp.)**
  - **Preliminary external detection efficiency: ~25% near 422nm**
  - **DCR a few kHz**
  - **Minimal interference from application of trapping-level RF**
- **Currently testing with ions**



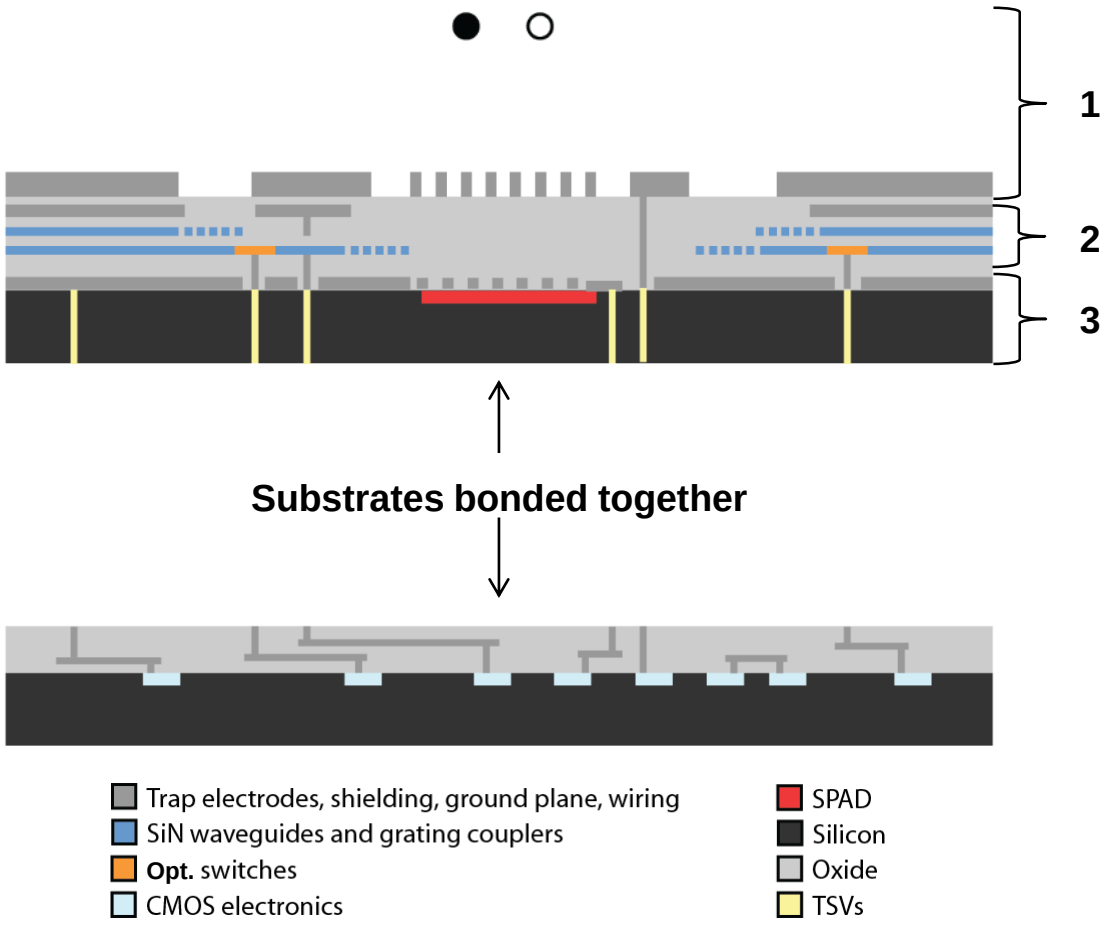
K.K. Mehta, PhD thesis (2017) [MIT]



Initial designs: Mehta, PhD thesis, MIT (2017)
Recent designs: Ryu, Donlon, Aull et al., unpublished (2021)

3D Integration of Optics and Control Electronics into Trap Chips

- **Top substrate**
  1. **Qubit layer**
     - **Ions**
     - **Electrodes**
  2. **Optical control layer**
     - **Waveguides**
     - **Grating couplers**
     - **Potential modulators**
  3. **Readout/transfer layer**
     - **APDs with grid/ITO**
     - **Substrate with TSVs**
- **Bottom substrate**
  - **Electronic control layer**
    - **CMOS, wiring, etc.**
- **Materials that allow for 3D integration are likely required**



ITO: Indium tin oxide
TSV: Through-substrate via

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  - Photon detection and 3D integration
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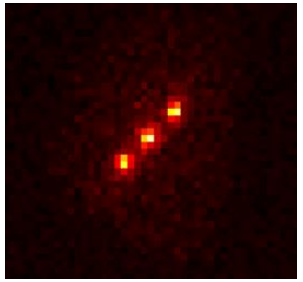
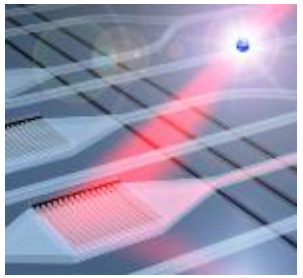
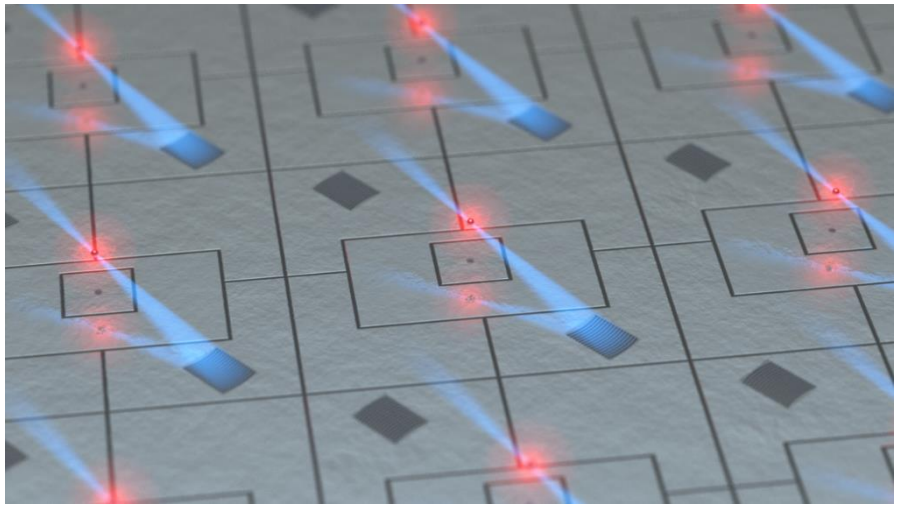




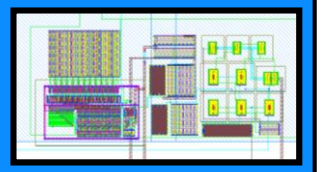
Integrated Electronics/Photonics for Sensor Platform

- Collaboration to develop portable optical clocks: ion arrays with integrated electronics
  - (Photonics integration along parallel path)
  - Electronics used to update trapping potentials to reduce systematic frequency uncertainties
  - Also to bias and read out integrated APDs
  - Sensor application: target room temperature
- Address power, speed, noise – tradeoff as required
  - More bits or DAC precision may be necessary
- On-chip programming based on measurements
- For QC, CMOS can be optimized for cryogenic operation
  - Design and fab must be altered

Concept for ion-array optical clock chip

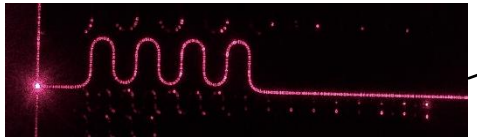


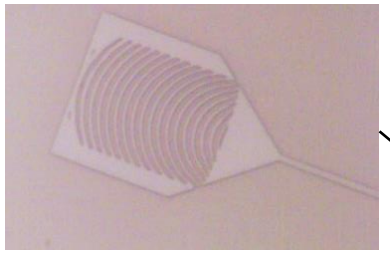
Integrated electronics for electrode potential control and APD biasing and readout

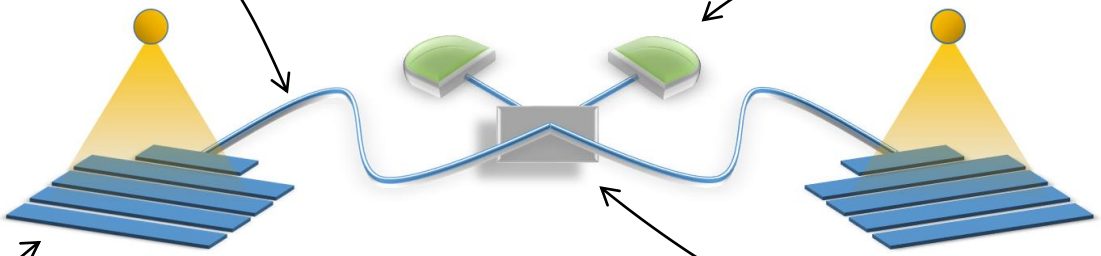


Integrated Collection for Remote Entanglement Generation

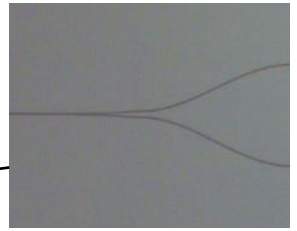
- **Integrated collection optics**
  - Collection grating to optimize light gathering of ion spontaneous emission
  - Based on emitting grating couplers, but tailored for a very different mode
  - REG on-chip; ions trapped separately; multiplex multiple ion sites to enhance speed
- **Working with Duke/SNL toward Ba^+ ion wavelength for on-chip collection (QSA)**
- **Also looking at Sr+ with UIUC (HQAN)**
- **Such collection could also allow waveguide coupling to detectors for state readout**







Detector can be on-chip or off

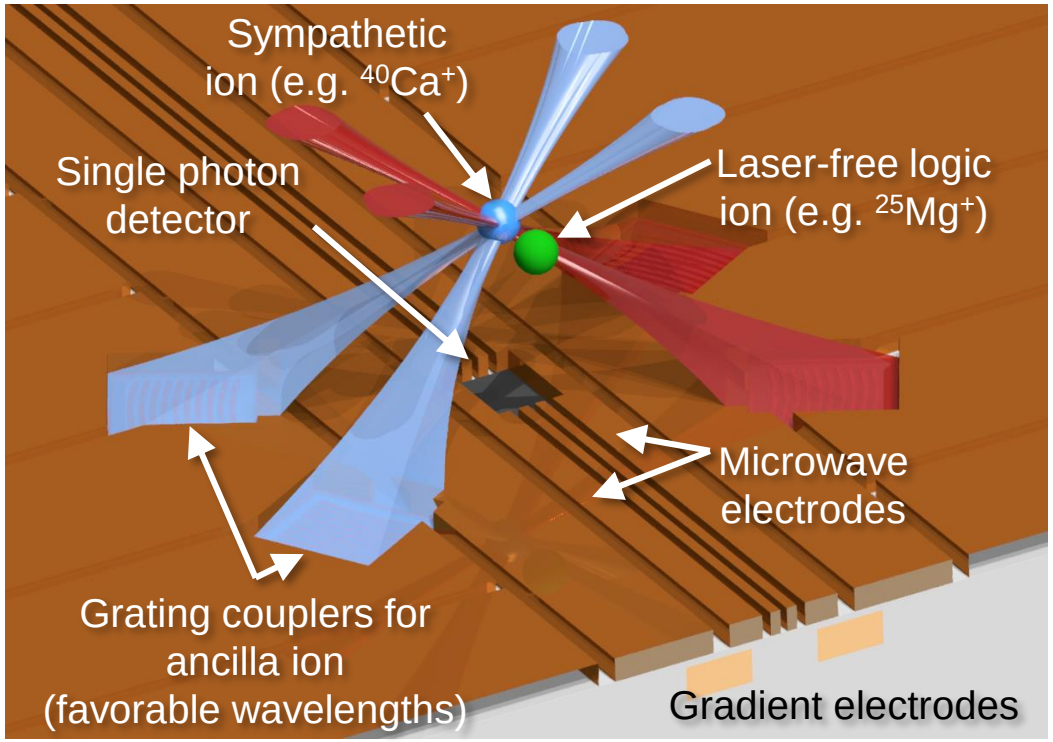


Options: Polarization or time-bin based entanglement

Integrated Dual-Species System for High-Coherence Computing and Sensing

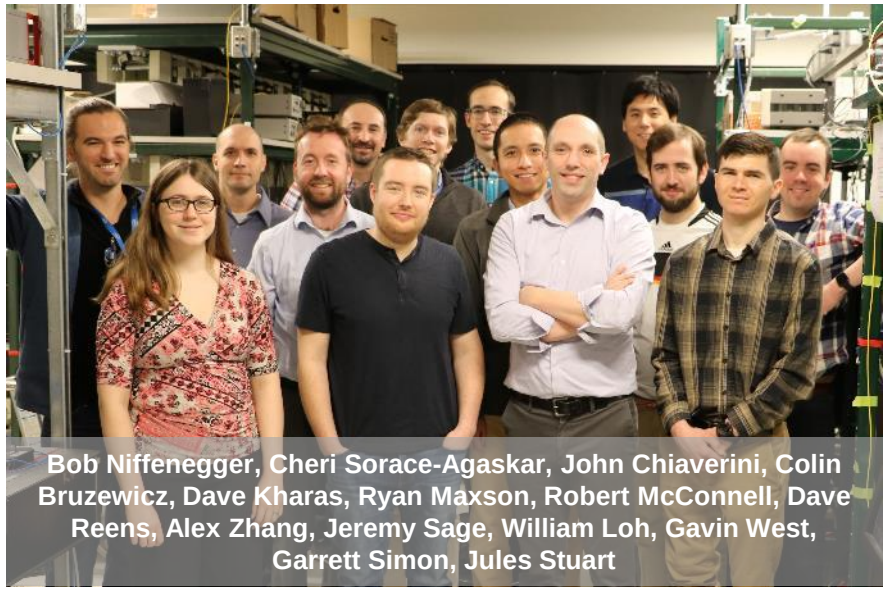
- Ca^+ is a great candidate for helper ion for a Mg^+ sensing/logic ion
  - Low, closely matched mass; good state detection; nice wavelengths
  - Mg^+ free from resonant optical fields
- Integrated optical elements for Ca^+ control
- Trap-integration of current carrying leads
- Gates using magnetic field gradients can avoid spontaneous emission
  - Precise RF electronics rather than lasers
- Detectors can be integrated for robust control with no free space optics

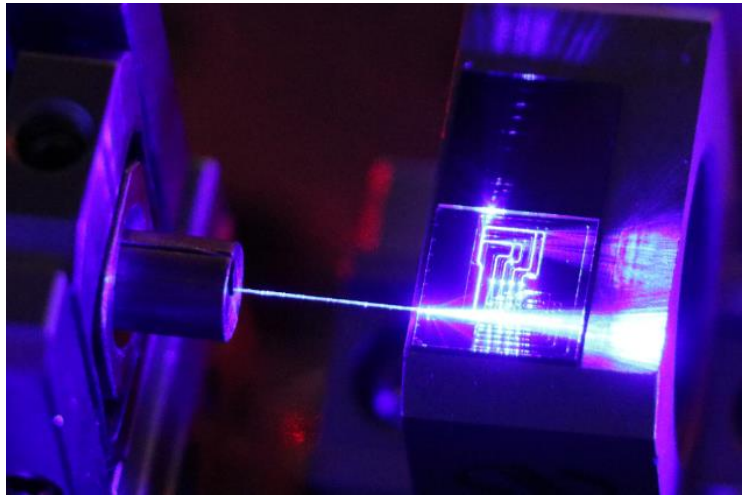
"All-Electronic Ion Qubit" concept incorporates multiple techniques and the integration of several technologies



High-fidelity RF gates: Srinivas et al., arXiv:2102.12533 (2021)
Integrated photo-detector: Todaro et al., PRL 126, 010501 (2021)

MIT-LL (and MIT) Ion Team


Bob Niffenegger, Cheri Sorace-Agaskar, John Chiaverini, Colin Bruzewicz, Dave Kharas, Ryan Maxson, Robert McConnell, Dave Reens, Alex Zhang, Jeremy Sage, William Loh, Gavin West, Garrett Simon, Jules Stuart



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- Jeremy Sage*
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- Reuel Swint
- Siva Yegnanarayanan

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- Kevan Donlon
- Kevin Ryu

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- Dave Kharas (also photonics)
- Peter Murphy
- Chris Thoummaraj

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- Paul Juodawlkis

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- Yuan Liu

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- Jules Stuart
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HQAN

Q-SEnSE

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