Versatile MRAM Technology

Sanjeev Aggarwal

2/10/2022

Safe Harbor Statement

Forward-Looking Statements

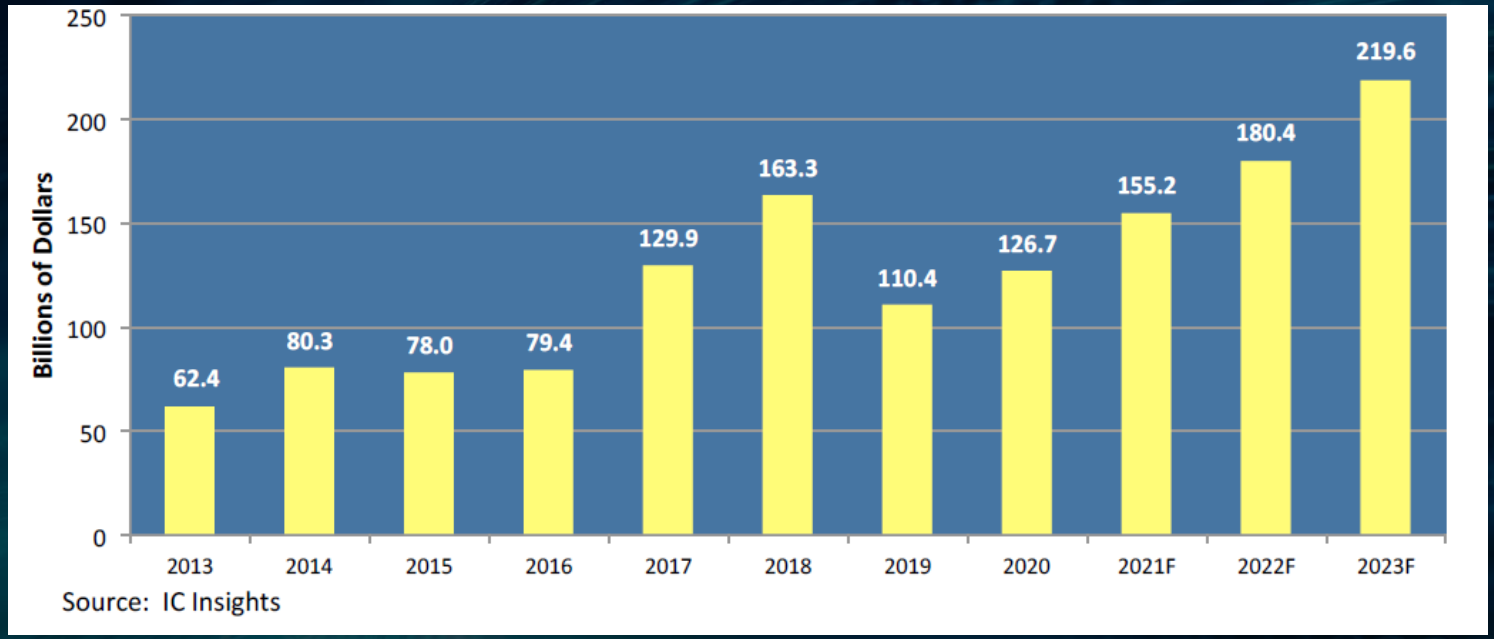
This presentation contains "forward-looking statements" that involve risks, uncertainties and assumptions. If the risks or uncertainties materialize or the assumptions prove incorrect, our results may differ materially from those expressed or implied by such forward-looking statements. All statements other than statements of historical fact could be deemed forward-looking statements, including, but not limited to: any estimates of addressable market size and our ability to capture that market, market trends and market opportunities, customer growth, product availability, technology developments, or other future events; any statements about historical results that may suggest future trends for our business; any statements regarding our plans, strategies or objectives with respect to future operations or business performance; any statements regarding future economic conditions; and any statements of assumptions underlying any of the foregoing. These statements are based on estimates and information available to us at the time of this presentation and are not guarantees of future performance. Actual results could differ materially from our current expectations as a result of many factors, including, but not limited to: market adoption of our products; our limited operating history; our ability to raise capital; our history of losses; our rate of growth; our ability to predict customer demand for our existing and future products; our ability to hire, retain and motivate employees; the effects of competition, including price competition; technological, regulatory and legal developments; and developments in the economy and financial markets.

We assume no obligation, and do not intend, to update these forward-looking statements, except as required by law.

Outline

- Memory market overview
  - Advantages of Magnetic Random Access Memory (MRAM)
  - MRAM Applications
- MRAM Technology
  - Toggle (Field switched) MRAM
  - Spin Transfer Torque MRAM (STT-MRAM)
- Versatility of MRAM Technology
- Summary & Future Direction

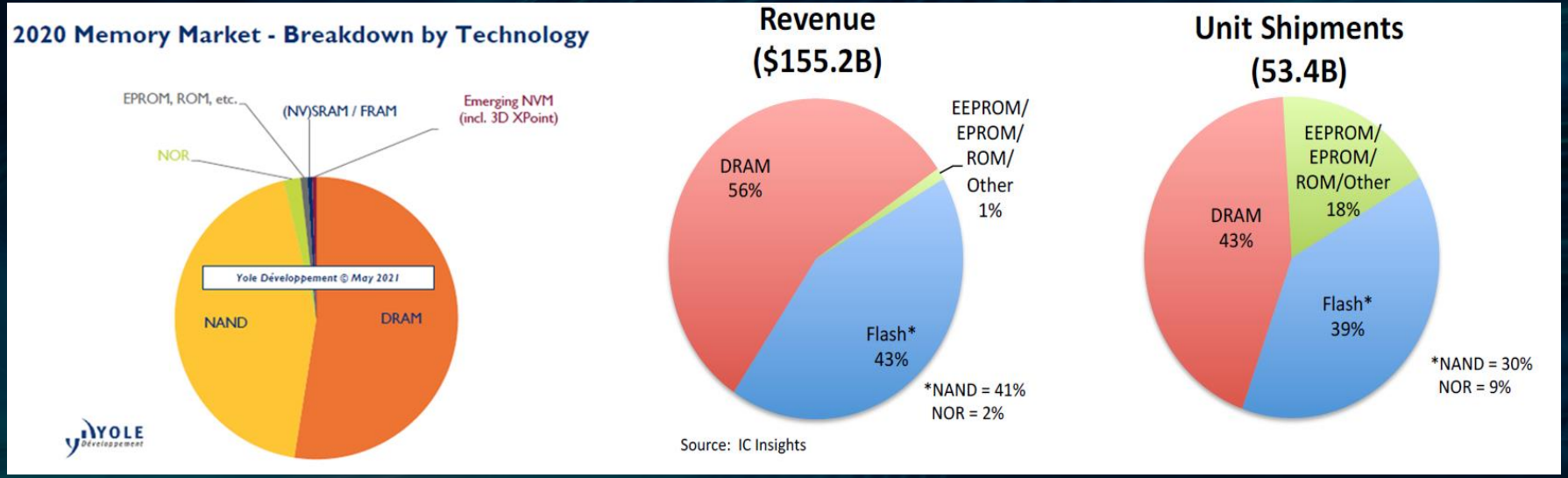
Semiconductor Memory IC Market ($B)



- After a steep drop in 2019, sales of memory ICs rebounded 15% during COVID-plagued 2020.
- Stronger DRAM pricing is expected to lift total memory revenue 23% in 2021 to $155.2 billion.

EVERSPIN TECHNOLOGIES

Semiconductor Memory Market 2021



- Dominated by DRAM and Flash. All other memories combined are <$5B.
- FRAM TAM= $303M, SRAM TAM= $450M, Traditional MRAM market targets
- NOR TAM= $2.3-3B, Target for higher density MRAM.

The MRAM Promise

PERSISTENCE

Maintains memory contents without requiring power

PERFORMANCE

SRAM & DRAM-like performance with low latency

ENDURANCE

Superior durability supports memory workloads without sophisticated management

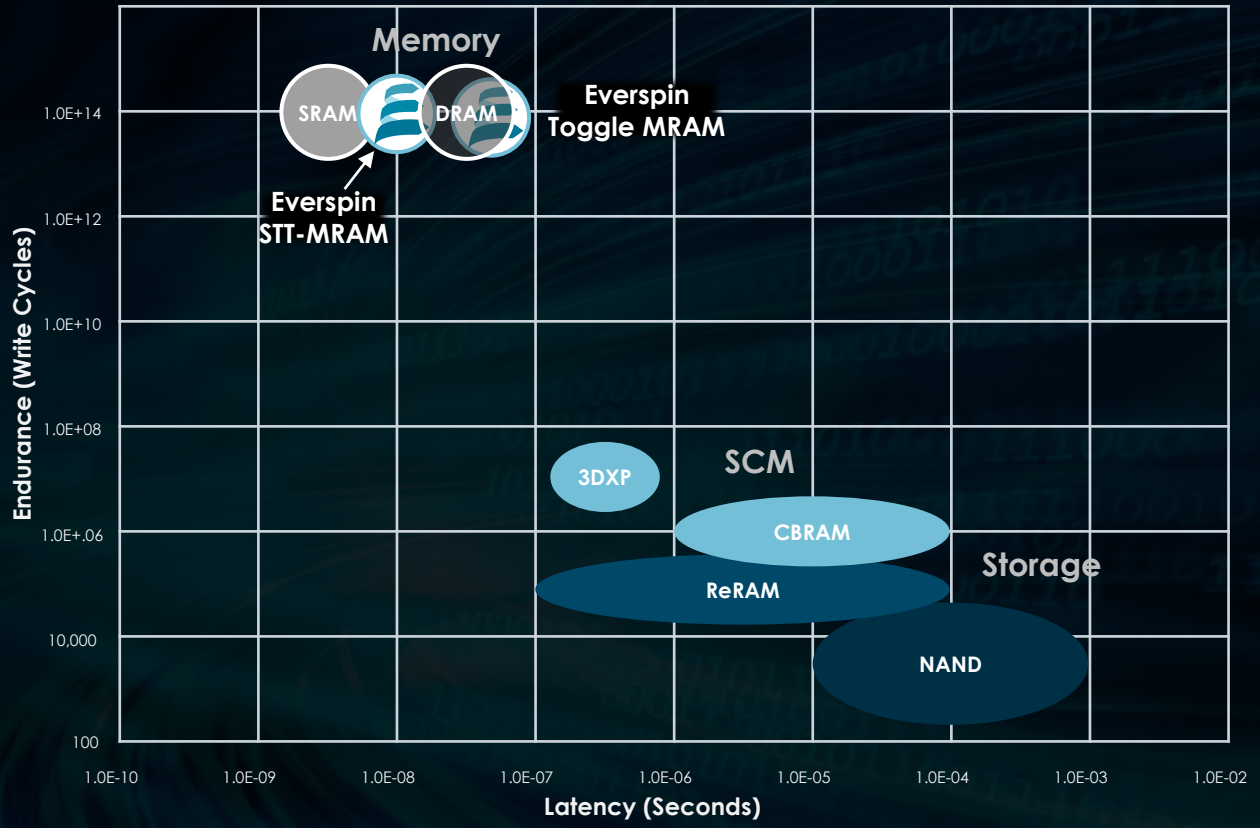
RELIABILITY

Best-in-class robustness designed and tested for extreme conditions

MRAM as a CPU-attached memory (like SRAM/DRAM) that brings non-volatile capability (like Flash)

EVERSPIN TECHNOLOGIES

MRAM Brings Native Persistence to Memory Workloads



MRAM COMBINES PERFORMANCE OF MEMORY WITH PERSISTENCE OF STORAGE

- **Persistence:** Months to decades of data retention without power or refresh
- **Performance:** Read/write similar to DRAM
- **Endurance:** Handles memory workloads

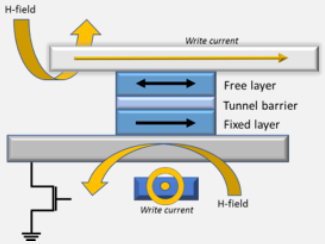
EVERSPIN TECHNOLOGIES

EVERSPIN®
TECHNOLOGIES

MRAM Technology

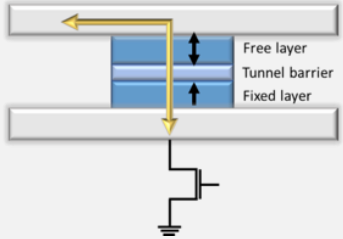
Technology Overview

Toggle (Field switched) MRAM



- In-plane magnetization
- Free layer switched with indirect magnetic fields
- Parallel and Anti-parallel states – 0 and 1
- Robust extended temperature reliability/operation
- Replacement for nvSRAM, FRAM, BBSRAM and NOR Flash

Spin Transfer Torque MRAM



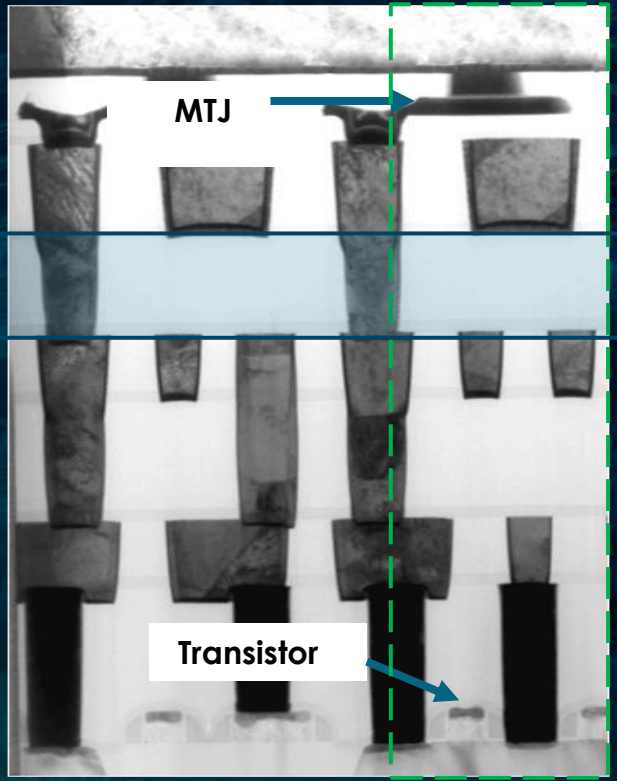
- Out of plane magnetization
- Free layer switched when current passes through the tunnel barrier
- Parallel and Anti-parallel states – 0 and 1
- Endurance and data retention are coupled
- High performance NVM with high chip capacity

Toggle MRAM X-section

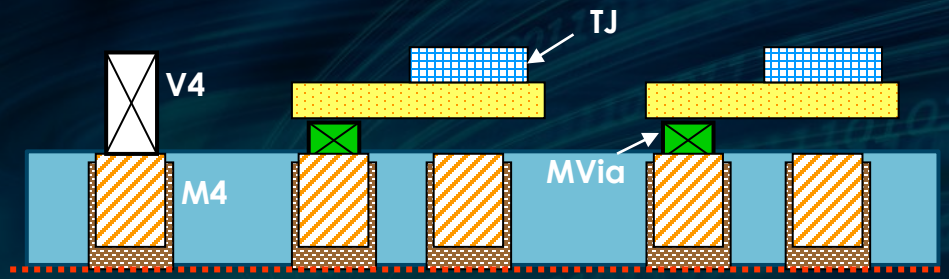
- MRAM Module integrated in the last 2 copper metal layers

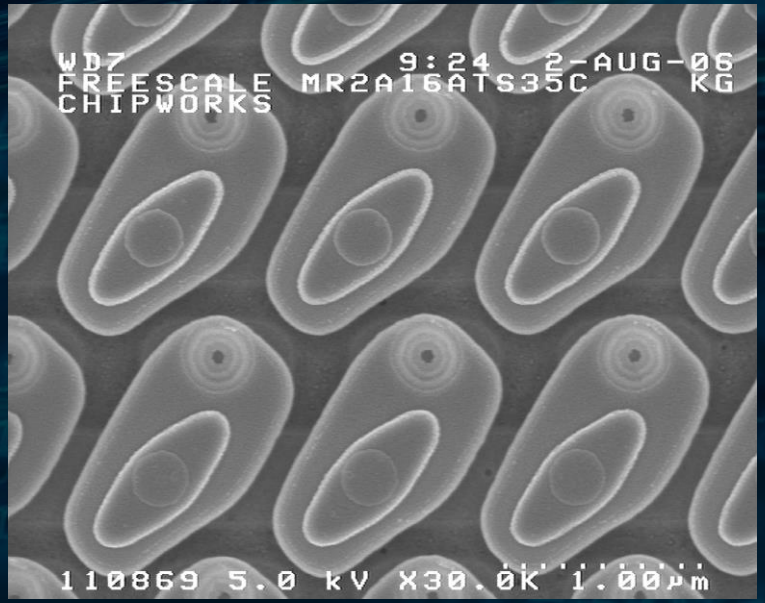
Transfer from foundry to Everspin

- CMOS up to Via2 processed in Foundry and shipped to Everspin to complete MRAM Module



Schematic of Toggle MTJ bit

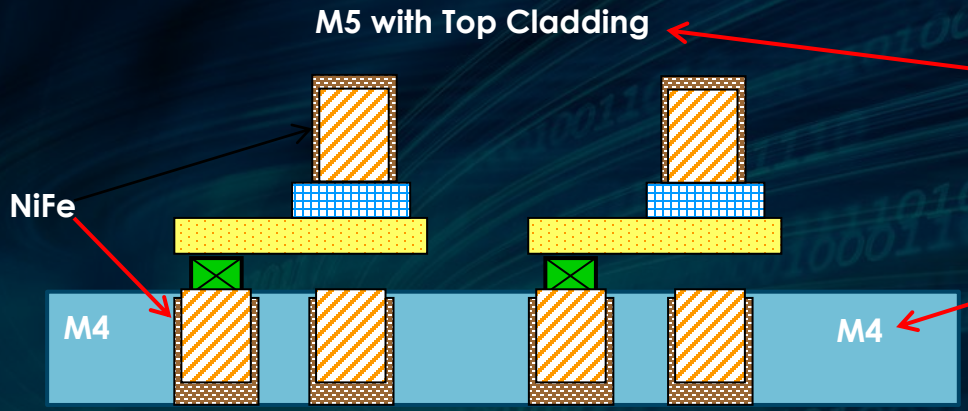


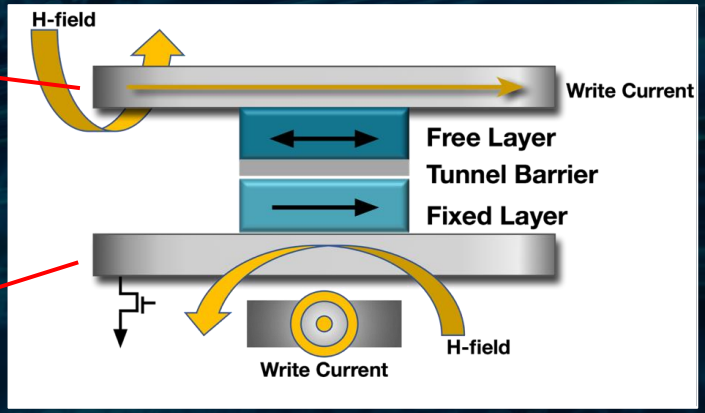


MRAM Layer Additions	MVia	BE	TJ	TC
	Msk1	Msk2	Msk3	Msk4

(Not shown)

Schematic of Field Switching Lines



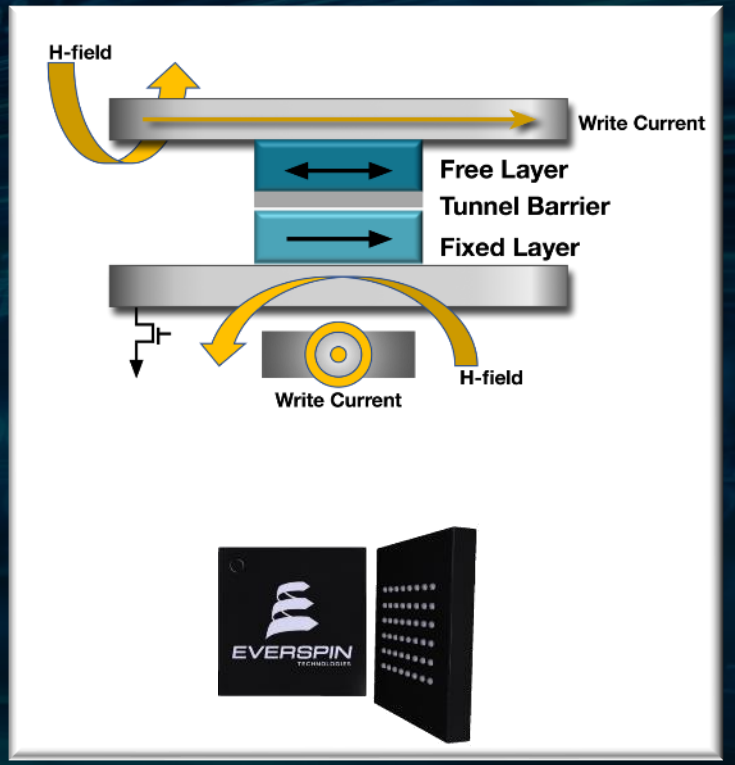


MRAM Layer Additions	MVia	BE	TJ	TC
	Msk1	Msk2	Msk3	Msk4

- NiFe films in the interconnect lines are used to generate magnetic fields to lower the bit switching current

Toggle MRAM Memory – The Ideal Non-Volatile Solution

- Near Unlimited Endurance, 20+ Year Data Retention, SRAM-Like Latencies
- Fastest non-volatile write – symmetrical Read/Write speeds and byte addressable
- Eliminates Storage Components
  - No need for Caps, Super caps and batteries
  - Allows power gating → zero standby power
- Pin compatible direct replacement
  - Standard parallel and serial (SPI) interfaces
  - Can replace SRAM, NVSRAM, BBSRAM, FRAM, E2PROM and NOR Flash



EVERSPIN TECHNOLOGIES

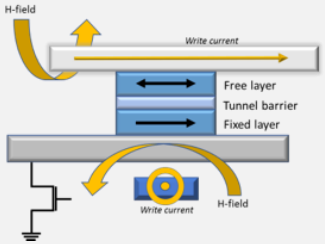
Toggle Solves System Challenges

	MRAM	BBSRAM	nvSRAM	Serial NOR	FRAM
Non-Volatile	Yes	Battery Required	V_{CAP} Required	Yes	Yes
Endurance	10^{15}	Limited by Battery	10^{6}	10^{5}	10^{13}-10^{15}
Retention	20+ yrs @125°C	Battery Life 4 –7 yrs @70°C	20 yrs @85°C	20 yrs @ 85°C	10 yrs @85°C
Parallel (ns)	35 – 45	15 – 100	25 – 45	>120 (read)	55 - 70
SPI (MHz)	50-104	50-108	50-104	133	50-108
External Charge	None	Battery	Capacitors	None	None
Temp Grade	Auto	Industrial	Auto	Auto	Auto for <2 Mb
Density	128Kb – 16Mb	8 Kb – 256 Mb	64 Kb – 16 Mb	4 Mb – 256 Mb	4 Kb – 8 Mb
Read Cycle	Non-destructive	Non-destructive	Non-destructive	Non-destructive	Destructive

EVERSPIN TECHNOLOGIES

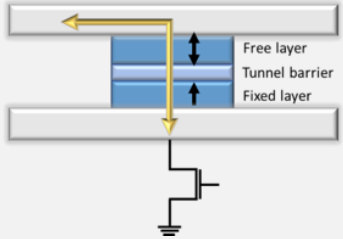
Technology Overview

Toggle (Field switched) MRAM



- In-plane magnetization
- Free layer switched with indirect magnetic fields
- Parallel and Anti-parallel states – 0 and 1
- Robust extended temperature reliability/operation
- Replacement for nvSRAM, FRAM, BBSRAM and NOR Flash

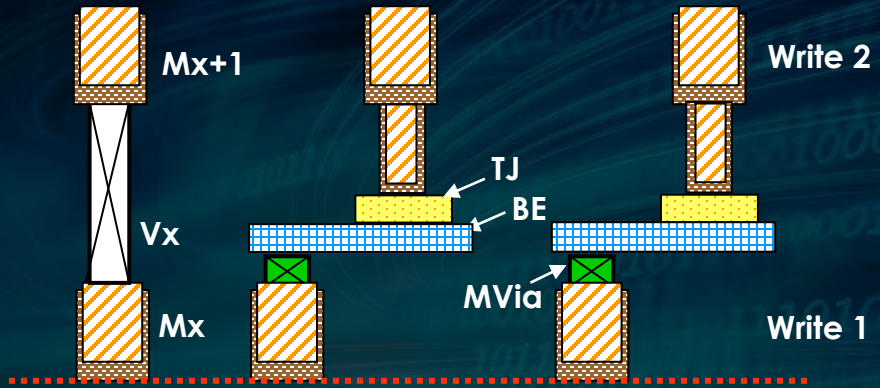
Spin Transfer Torque MRAM



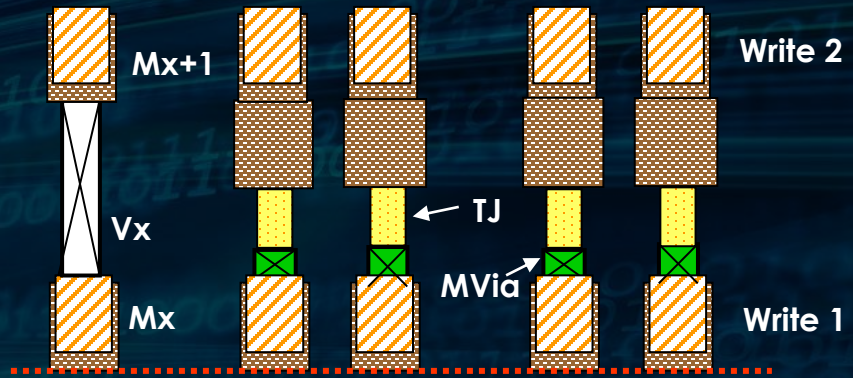
- Out of plane magnetization
- Free layer switched when current passes through the tunnel barrier
- Parallel and Anti-parallel states – 0 and 1
- Endurance and data retention are coupled
- High performance NVM with high chip capacity

STT-MRAM – Easy to Integrate with Standard CMOS

Off Axis Integration



On Axis Integration



MRAM Layer Additions

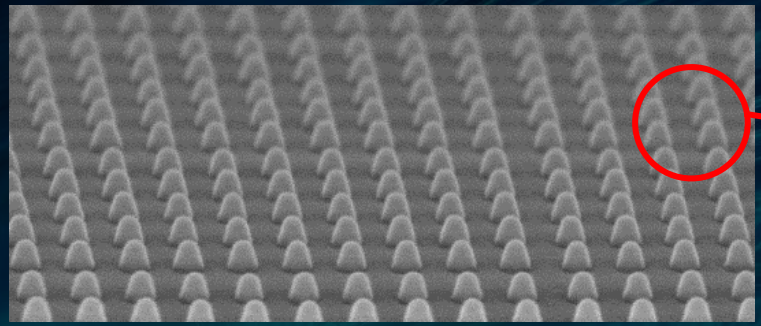
MVia Msk1 | TJ Msk2 | BE Msk3 | TJVIA Msk4

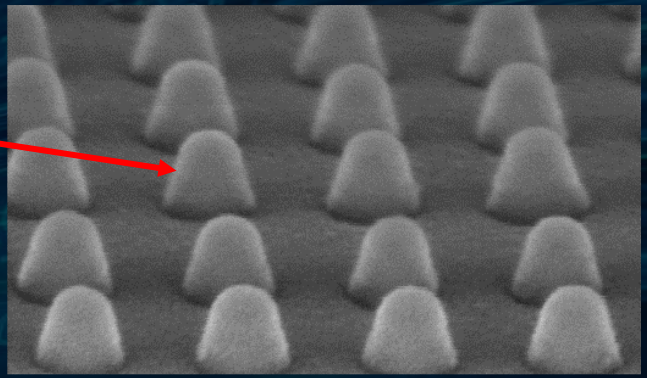
MRAM Layer Additions

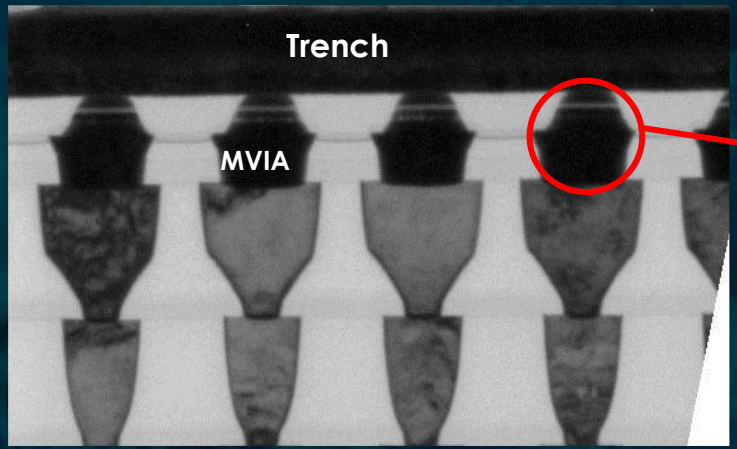
MVia Msk1 | TJ Msk2 | Trench Msk3

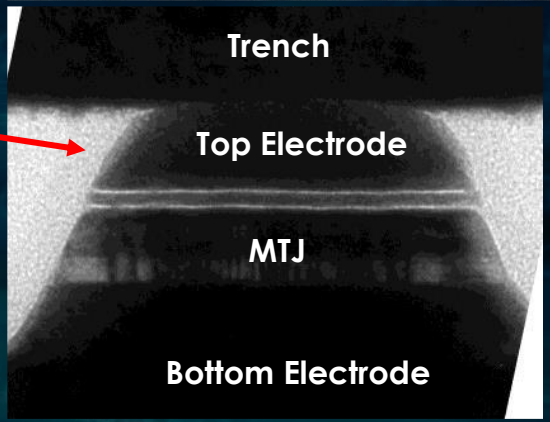
EVERSPIN TECHNOLOGIES

STT-MRAM Integration









EVERSPIN TECHNOLOGIES

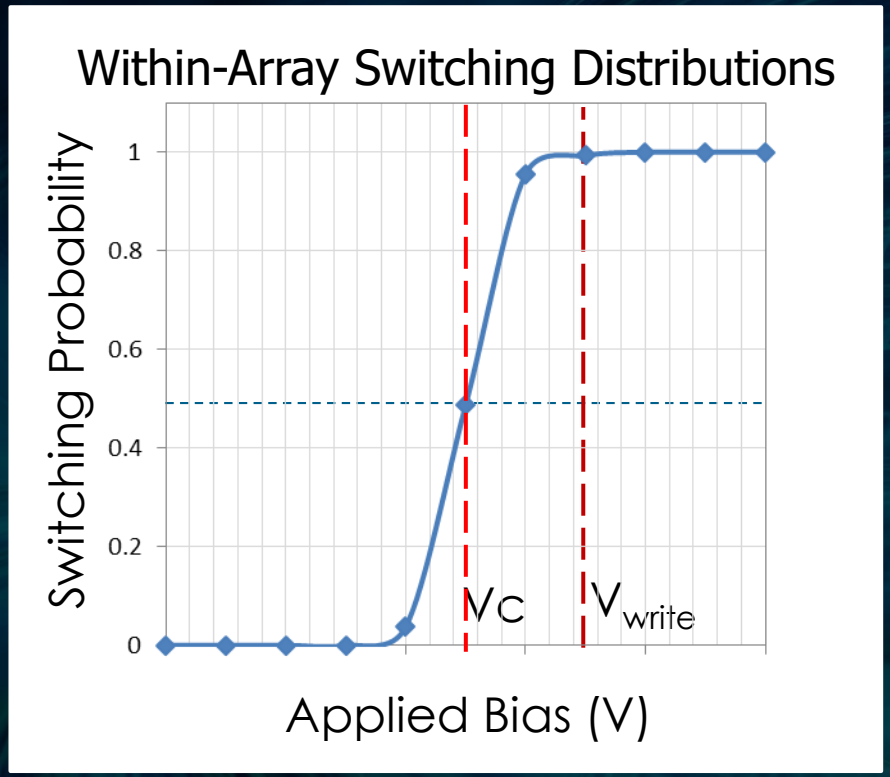
Key requirements for commercial MRAM technology

- Reliable read: High MR and narrow resistance distributions
- Reliable write: Well-behaved switching distributions
- Data retention: High energy barrier (Eb) and narrow distribution
- Cycling endurance:
  - STT-MRAM requires large separation between write and breakdown
    - Low Vc, high Vbd, and narrow, well-behaved distributions for both
- Extrinsic: Need very low level of magnetic and electrical extrinsic bits
  - For narrow, well-behaved distributions

Key requirements for commercial MRAM technology

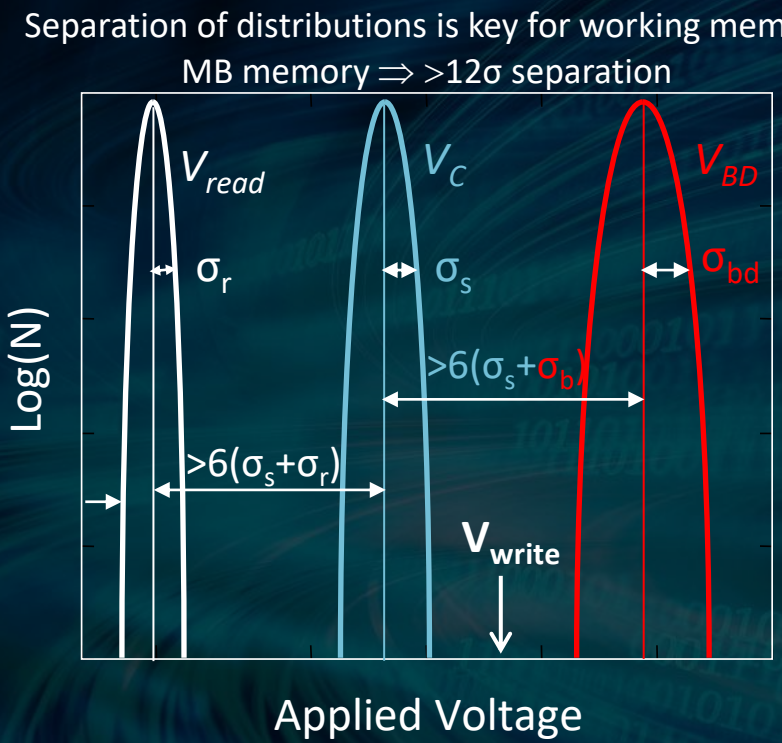
- Reliable read: High MR and narrow resistance distributions
- Reliable write: Well-behaved switching distributions
- Data retention: High energy barrier (Eb) and narrow distribution
- Cycling endurance:
  - STT-MRAM requires large separation between write and breakdown
    - Low Vc, high Vbd, and narrow, well-behaved distributions for both
- Extrinsic: Need very low level of magnetic and electrical extrinsic bits
  - For narrow, well-behaved distributions

Vc Distribution Determines Write Operating Voltage



- Vc is the voltage required to switch half the bits in an array
- To achieve low write error rate (WER), the required applied voltage for write, V_{write}, is higher than Vc

Must Separate bit-to-bit Distributions in the Array



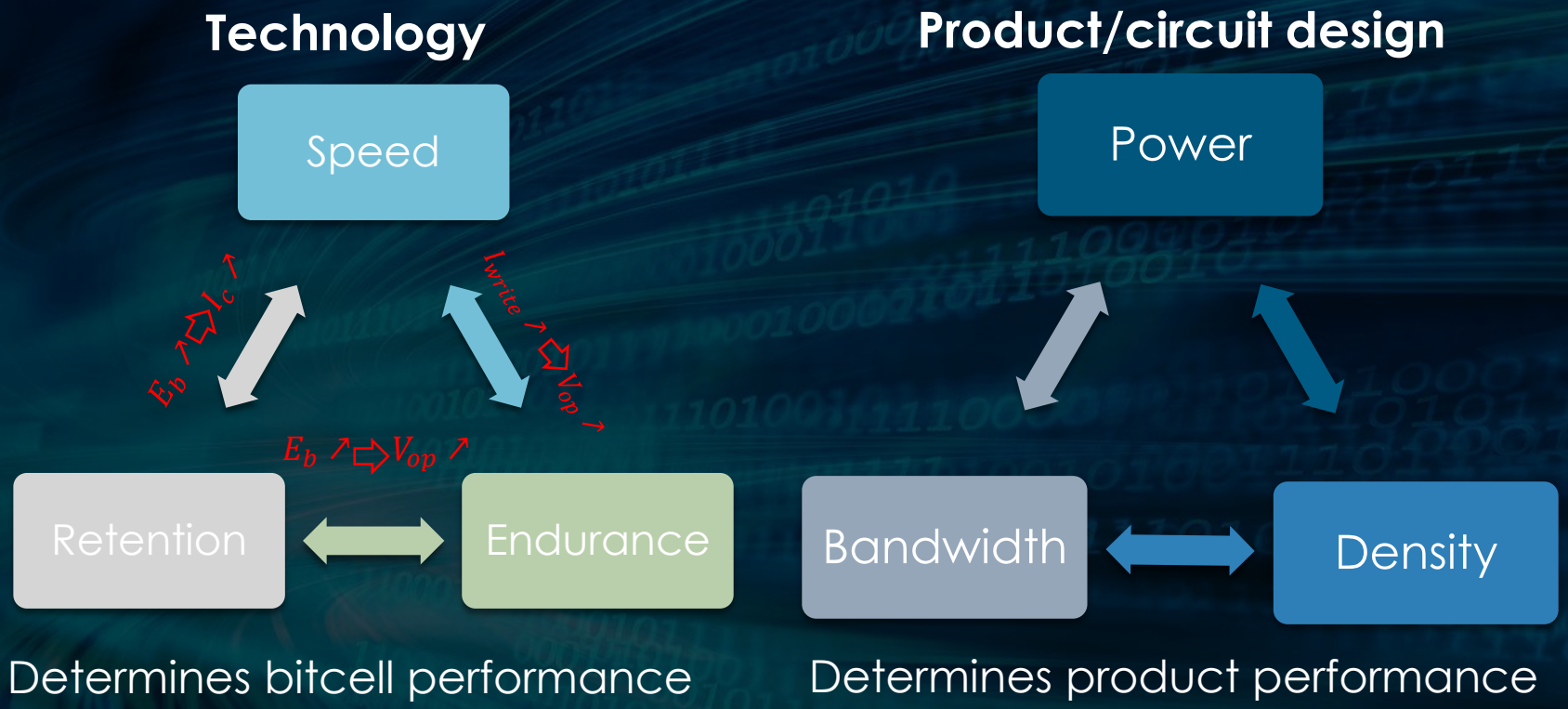
- Separation of V_C & V_{BD}
  - V_{write} must be well above V_C and well below V_{BD}
  - Tight switching distributions
  - Tunnel barrier reliability
- Separation of V_{read} & V_C
  - Avoid read-disturb errors
  - Bigger issue for smaller bits, lower I_C
- Separation gets worse with:
  - Shorter write pulses
  - Smaller bits
  - Extrinsic switching or breakdown behavior

EVERSPIN TECHNOLOGIES

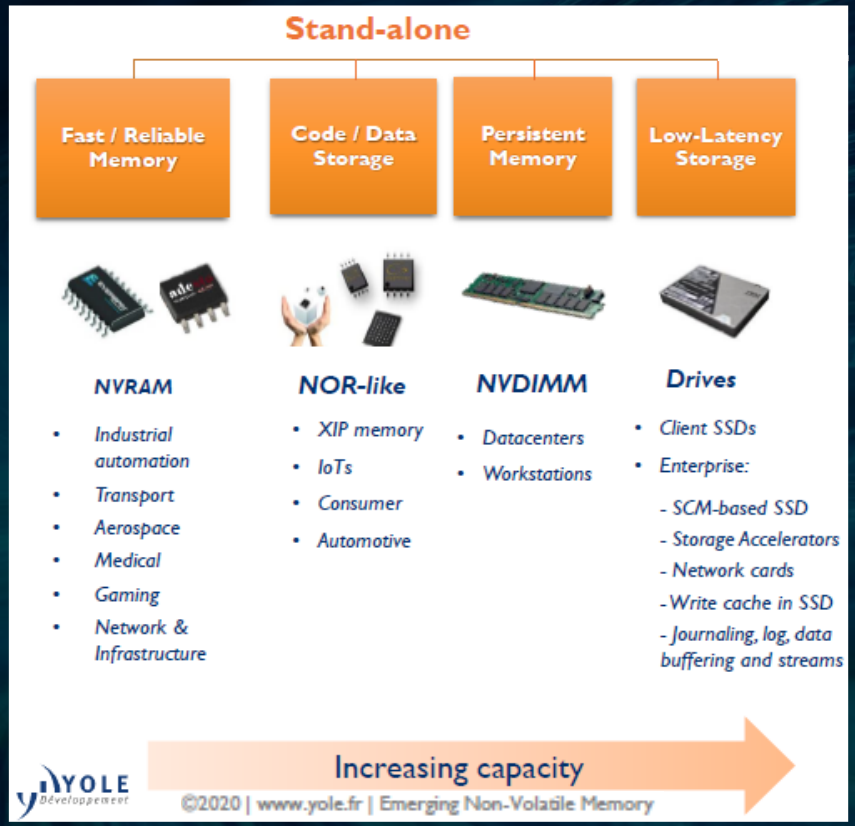
EVERSPIN®
TECHNOLOGIES

Versatility of MRAM Technology

STT-MRAM Design and Technology Solution



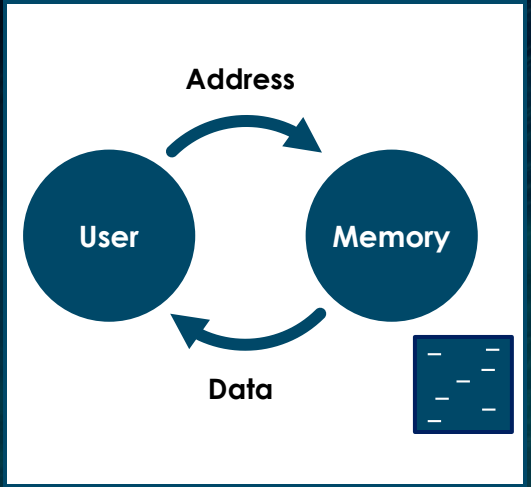
MRAM Standalone Product Family



- The same technology can address multiple products by optimizing the Technology and Product / Circuit design
- Required array performance: 10-20ns read, 20-50ns write achieved thru Technology
- Reliability will be determined by the memory array achieved thru Technology
- End-user performance is often determined by Product / Circuit design

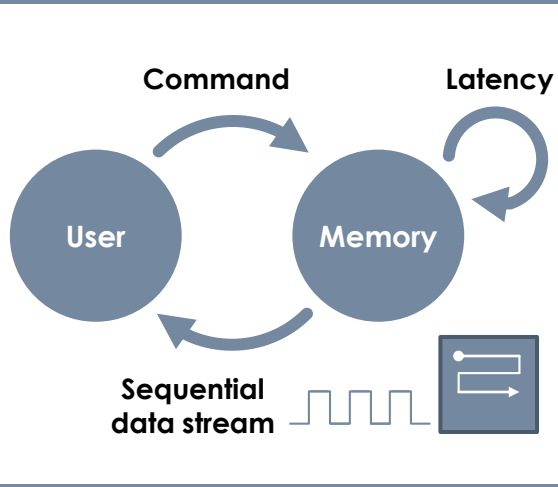
Memory Interfaces for MRAM

Parallel



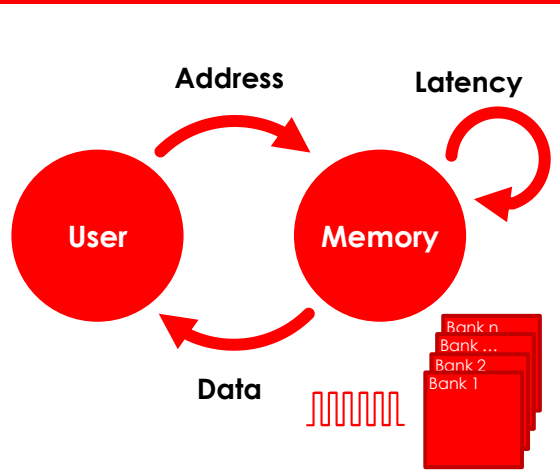
- Simple
- High pin count for bandwidth

Serial (xSPI)



- Simple
- Low pin count/small package
- Flexible (used for RAM, NOR and NAND)

Double Data Rate (DDR)

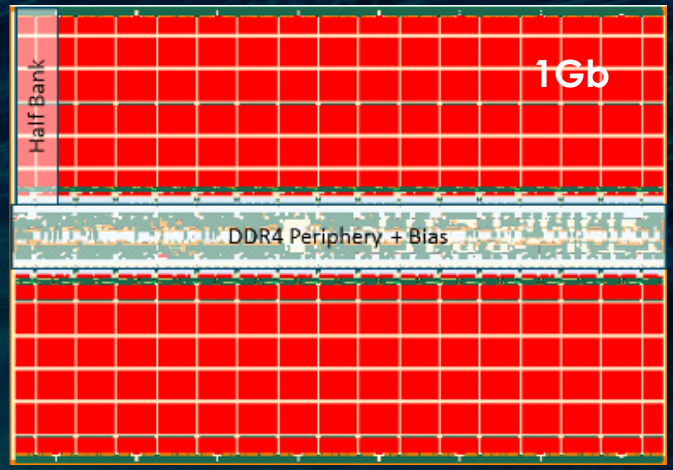


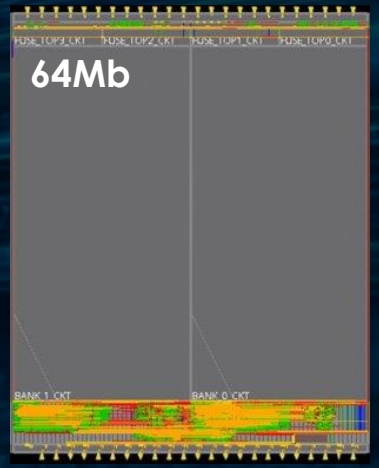
- Complex
- Optimized for DRAM and high bandwidth

EVERSPIN TECHNOLOGIES

Similar MTJ with Different I/F – Data Center and Industrial Markets

	1Gb ST-DDR4	64Mb xSPI
Supply voltage	1.2V	1.8V
Clock frequency	667 MHz	Up to 200 MHz
Number of IOs	16	1,4,8
Bandwidth	2.6 GB/s	Up to 400 MB/s
Temperature range	0°C to +85°C	-40°C to +85°C
Data retention	70°C 3mo	85°C 10yr
Endurance	>1e10 cycles	>1e15 cycles
Bit Error rate	<1e-11	<1e-15
Package	10x13	6x8

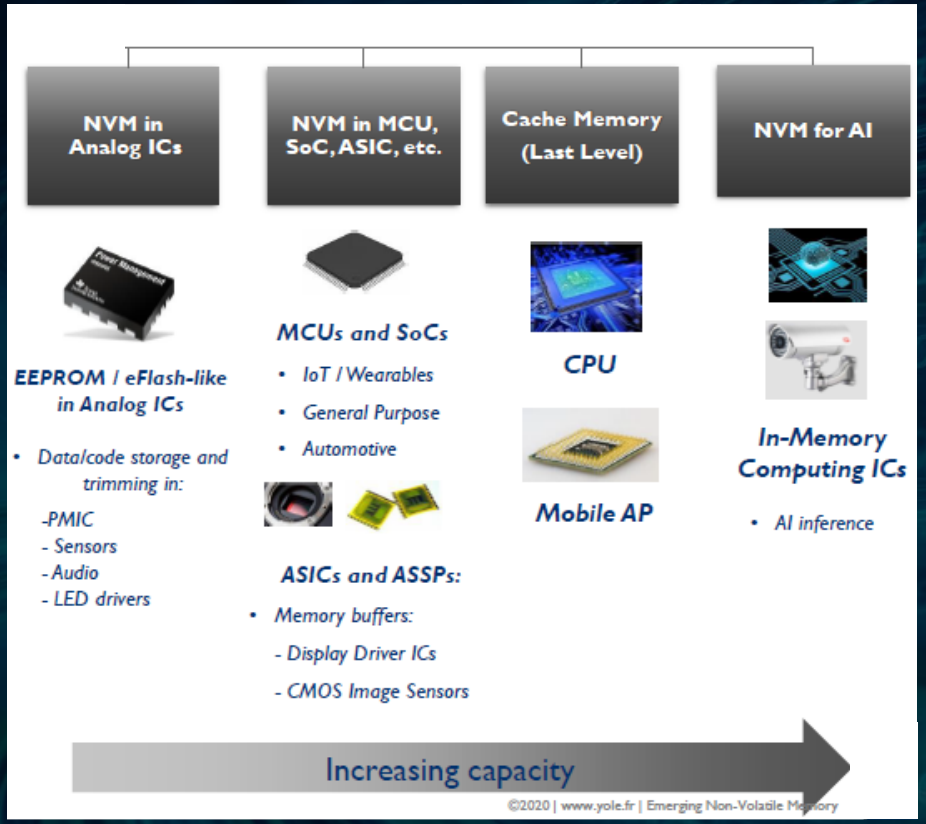




- **DDR**: data center applications / high bandwidth, high density
- **xSPI**: industrial market / lower density, lower speed but stringent reliability
- Both products are built on GlobalFoundries 28nm CMOS

EVERSPIN TECHNOLOGIES

MRAM Embedded Product Family



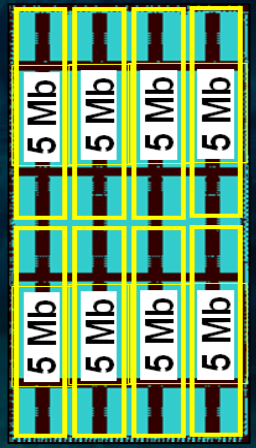
- Currently available eMRAM solutions are focused on code storage for eFLash replacement
- Value proposition for next gen eMRAM is all about density and speed to replace eDRAM/SRAM
- Retention is less important and can be traded off for better high speed write performance
- Feasibility of MRAM for cache applications is yet to be proven
- Read/write speed and endurance requirements are very challenging
- 5ns read, 5ns write
- Extremely low BER

EVERSPIN TECHNOLOGIES

GF – eMRAM macro on 22nm FD-SOI

1T-1MTJ bit-cell (Cell size ~0.047 um²)	
Specification Items	**Product Spec**
Temperature	-40~125 °C
Array size	40Mb
Solder Reflows	260 °C 5x Reflows
Read Access Time	19 ns (excl. ECC)
Write Cycle Time	200 ns
IO Width	64b+14b ECC
Power Supply	0.8V / 1.8V
ECC	2bit-ECC
Data Retention	>20 years, 0.1 PPM
Endurance	100K cycles
AMI @ 1 PPM	±250 Oe
SMI @ 0.1 PPM, (Median-3σ)	≥ ±450 Oe @125°C

- 40Mb eMRAM macro with 5x Solder Reflows compatibility is qualified for industrial-grade applications
- Macro includes internal bias generator, temperature and timing control and 2-bit ECC options



Source GlobalFoundries™

EVERSPIN TECHNOLOGIES

MRAM Products – Available and To Be Announced

Maker	Everspin				Global-Foundries	TSMC	Samsung	Intel	Avalanche
Product	Toggle MRAM standalone	STT-MRAM standalone			STT-MRAM embedded				STT-MRAM standalone
Memory capacity	**128kb – 32Mb**	**256Mb**	**1Gb**	**8Mb – 256Mb**	**40Mb**	**10Mb**	**8Mb**	**7.2Mb**	**8Mb – 16Mb**
Application or interface	Serial peripheral interface or parallel interface	ST-DDR3	ST-DDR4	Serial peripheral interface	eFlash replacement	eFlash replacement			Serial peripheral interface or parallel interface
Si technology	180 nm, 130 nm	40 nm	28 nm	28 nm	22 nm	22 nm	28 nm	22 nm	40 nm

- The standalone products have several different interfaces
- Embedded products mainly aim at replacing embedded NOR flash memory
- New stand-alone STT-MRAM products will arrive soon: lower latency, unlimited endurance cycles, and industrial grade data retention

EVERSPIN TECHNOLOGIES

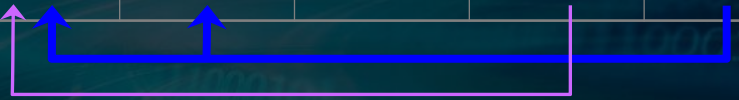
EVERSPIN® TECHNOLOGIES

Summary & Future Direction

Comparison of MRAM with Other Memories

In Development

	SRAM	DRAM	3D NAND Flash	**Toggle-MRAM**	**STT-MRAM**	ReRAM	PCRAM	FeFET	NRAM (CNT)
Nonvolatility	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Endurance (cycles)	Unlimited	Unlimited	$10^3 – 10^5$	Unlimited	$10^9 – 10^{12}$ Unlimited	10^5 - 10^9	$10^6 – 10^9$	10^4 - 10^5	10^{15}
Write speed (ns)	< 1	1 – 10	$10^5 – 10^6$	1-10	1 – 100	10 - 10^5	100 - 10^4	10	10
Memory capacity	Small – Medium	Large	Large	Small	Medium	Small – Large (demo 32Gb)	Medium – Large	Small (demo 32Mb)	Small (demo 16Mb)

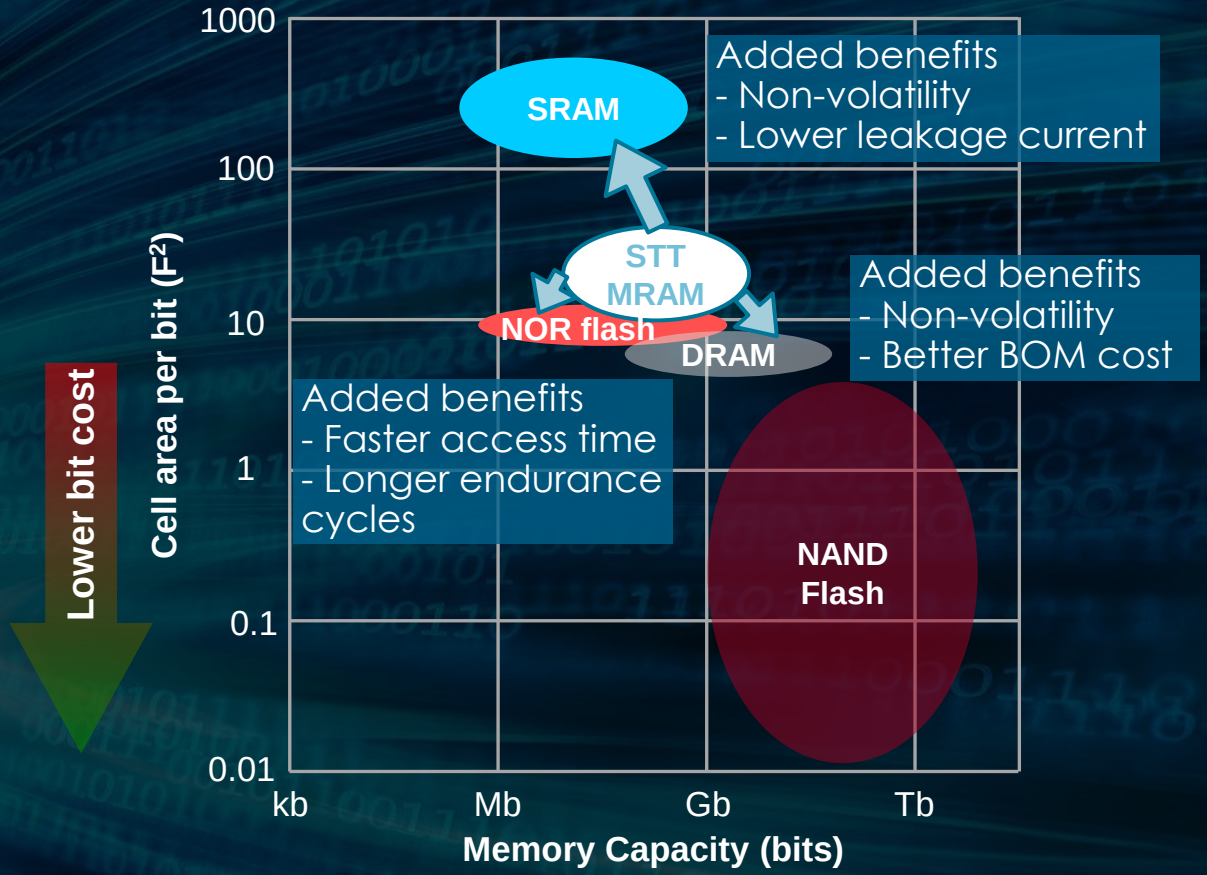


- Among new memories: MRAM, ReRAM, and PCRAM,
  MRAM has longer cycling endurance and faster write → SRAM or DRAM like usage

EVERSPIN TECHNOLOGIES

Future Adoption of STT-MRAM

- Bit cost is governed
  - By cell area
  - Wafer cost
  - Cost of ownership
  - Yields, etc.
- STT-MRAM offers several advantages over standard memories
  - Adoption based on value add
  - BOM cost instead of bit cost
  - System solutions (partial replacement)



EVERSPIN TECHNOLOGIES

Acknowledgements

- **Colleagues at Everspin Technologies**

  M. Arora, M. DeHerrera, B. Hughes, S. Ikegawa, H. K. Lee, F. B. Mancoff, S. Mukherjee, G. Shimon, J. J. Sun, A. Shah, S. M. Alam, D. Houssameddine, K. Nagel

- **Partners for STT-MRAM Manufacturing & Development**

GlobalFoundries™

EVERSPIN® TECHNOLOGIES