Fraunhofer IPMS

Fraunhofer Institute for Photonic Microsystems IPMS

Microelectronics meets Quantum Computing
An Overview of Fraunhofer IPMS' Approach

NY CREATES Seminar, May 2024

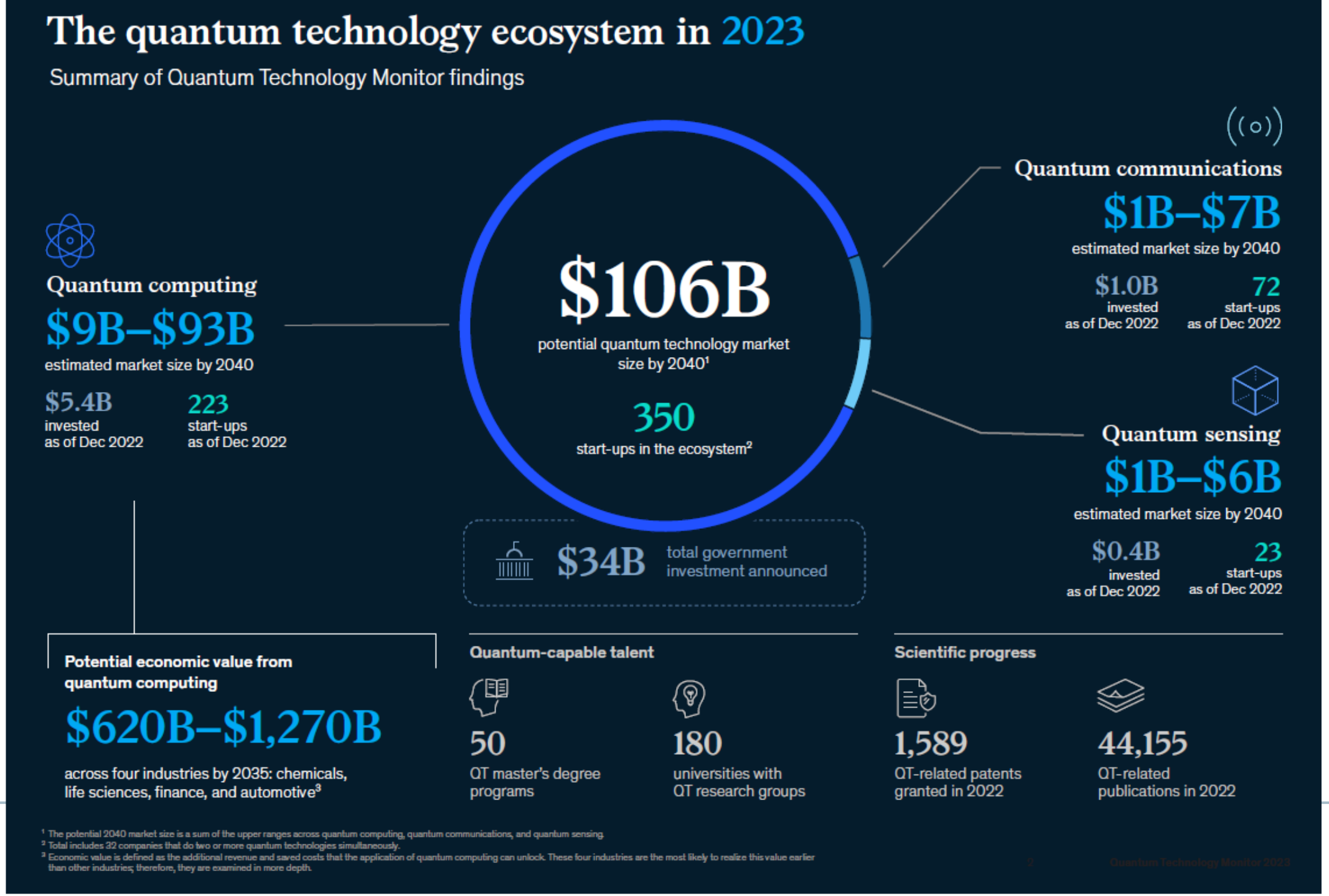
Dr. Benjamin Lilienthal-Uhlig
Fraunhofer IPMS

- Quantum Computing ?!
- Impressions on current State of Play
- Challenges… → Microelectronics ?
- Short interlude about Fraunhofer
- Solutions & ideas & Some examples
- European strategy

Quantum Computing ?!

The quantum technology ecosystem in 2023

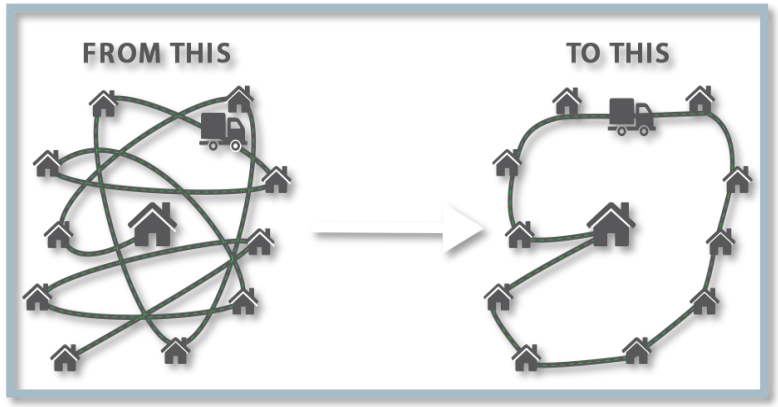
Summary of Quantum Technology Monitor findings

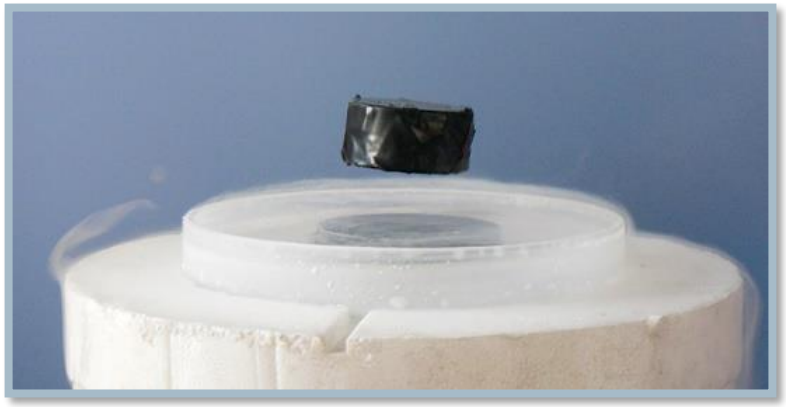


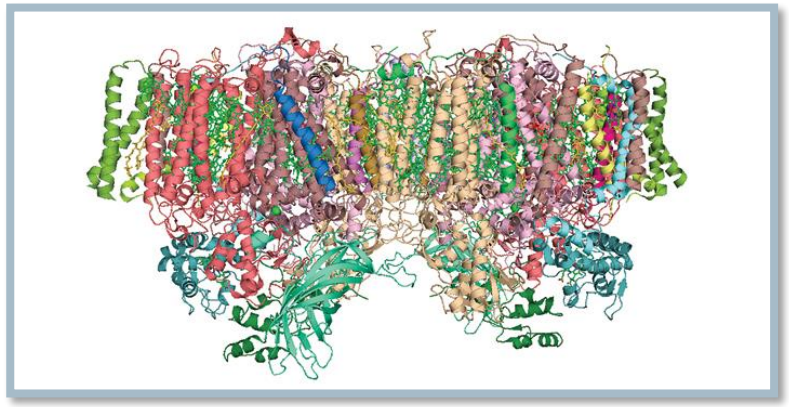
[1] The potential 2040 market size is a sum of the upper ranges across quantum computing, quantum communications, and quantum sensing.
[2] Total includes 32 companies that do two or more quantum technologies simultaneously.
[3] Economic value is defined as the additional revenue and saved costs that the application of quantum computing can unlock. These four industries are the most likely to realize this value earlier than other industries; therefore, they are examined in more depth.

Applications in the future

- Medical and Health
- Material Science
- Logistics and Traffic
- Finance
- …

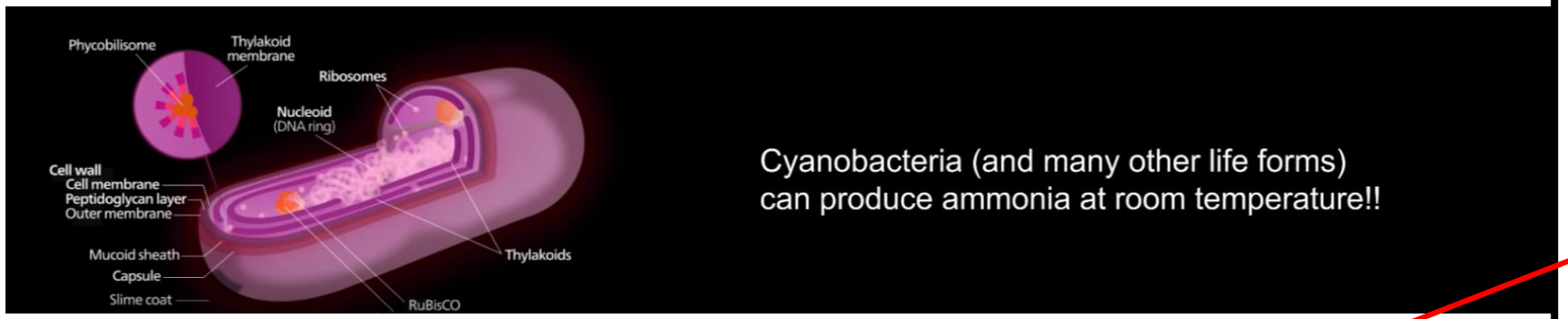




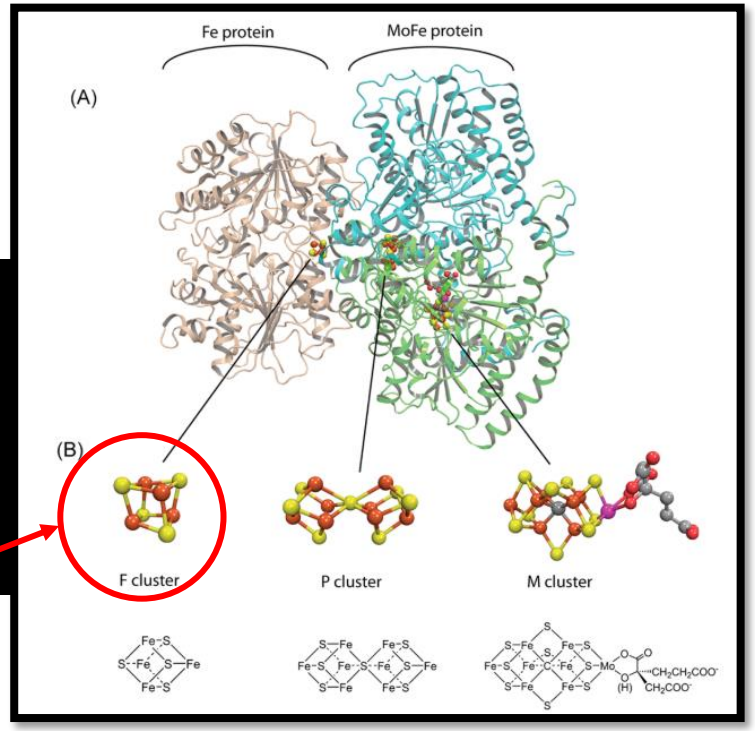


Example from Quantum Chemistry

Low efficiency
High energy consumption

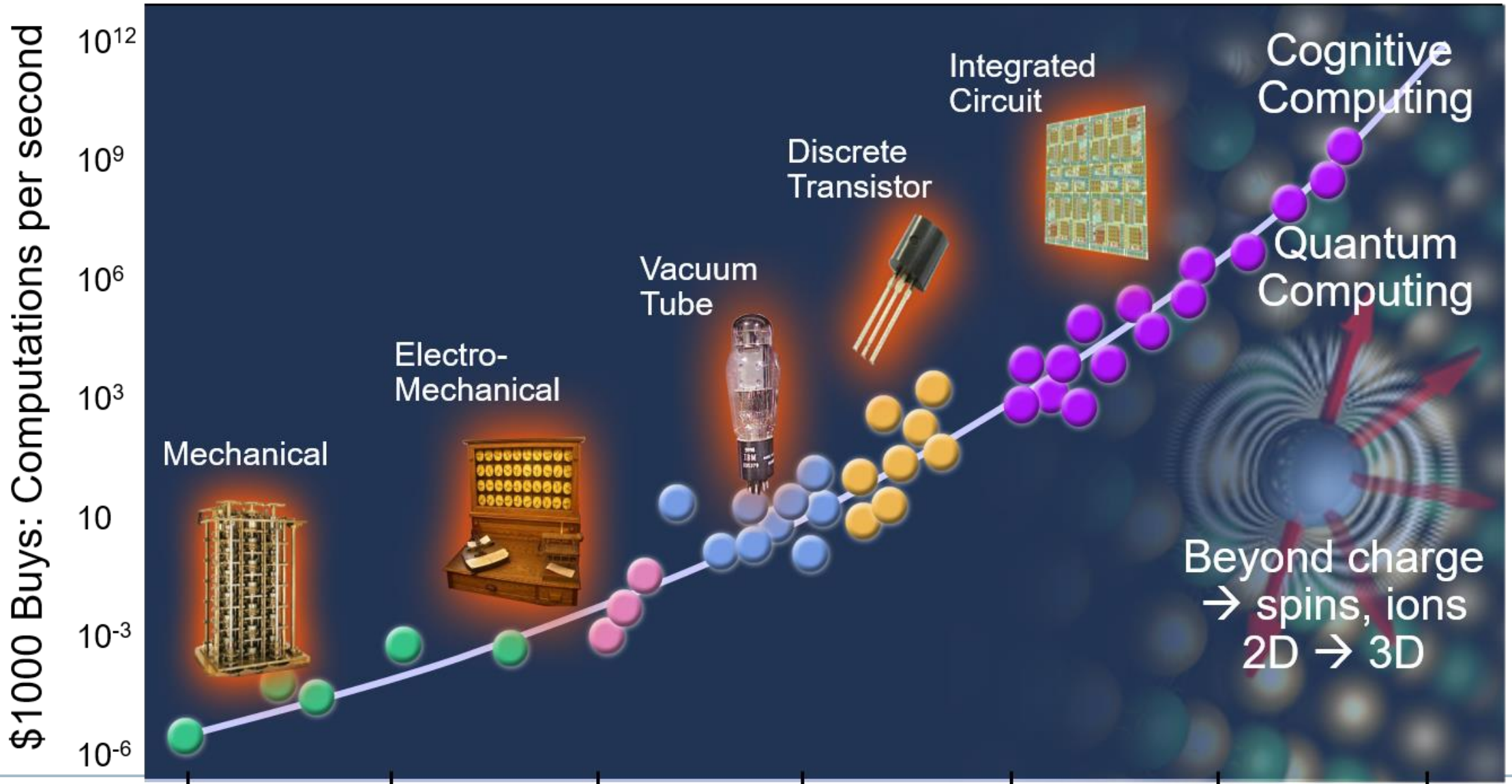


Cyanobacteria (and many other life forms)
can produce ammonia at room temperature!!



Only this can be simulated classically

Technology Eras - Computing



Source: Kurzweil 1999 – Moravec 1998

7

How we did, do or will compute

Big Picture

Abacus (2500 BC)

analog

deterministic

sequential

usefull

Classical computer (1950)

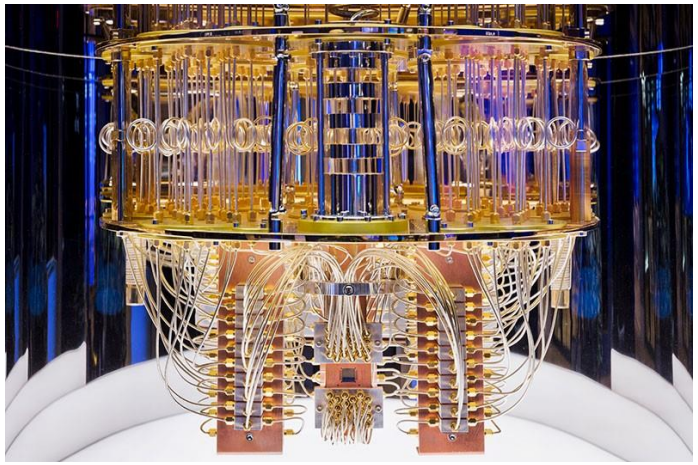
digital

deterministic

sequential

really usefull !

Quantum computer (20xy)



somehow digital, but it‘s complicated

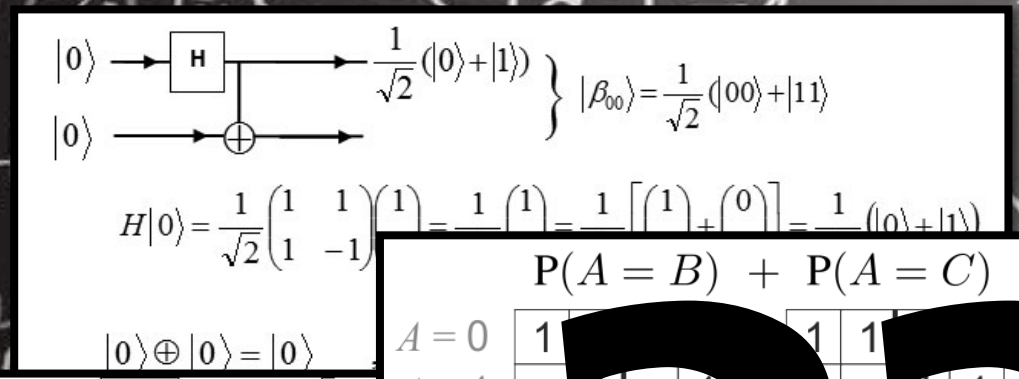
‚probabilistic‘

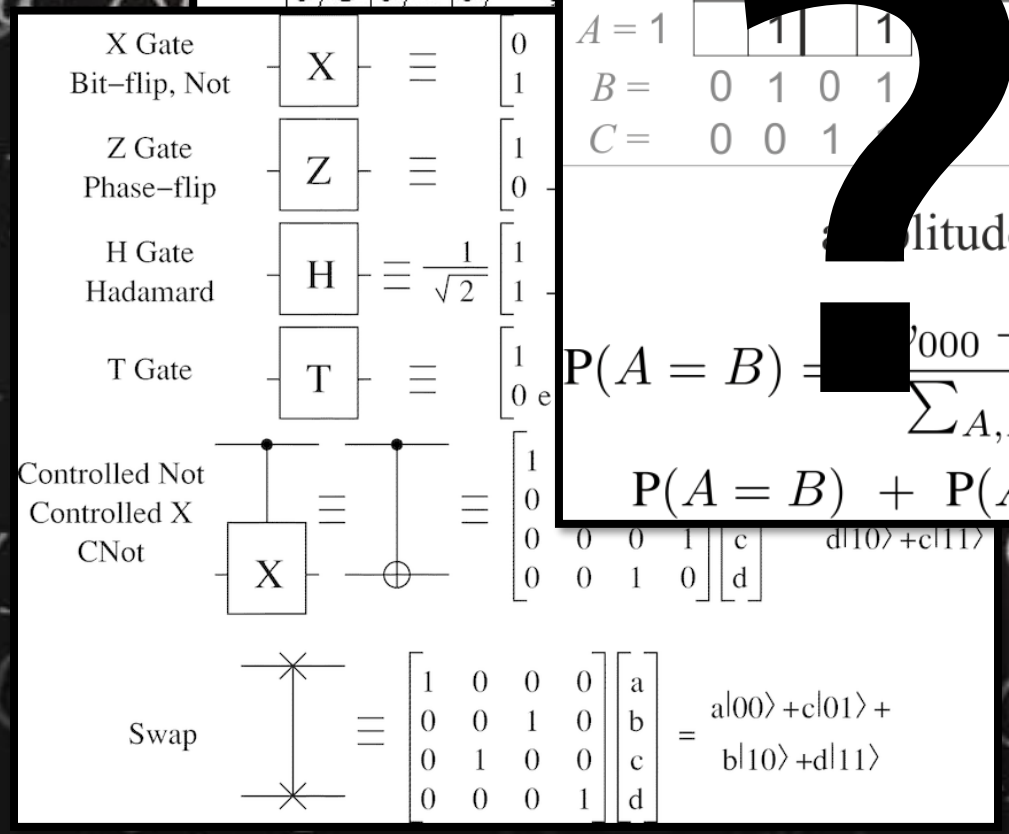
parallel

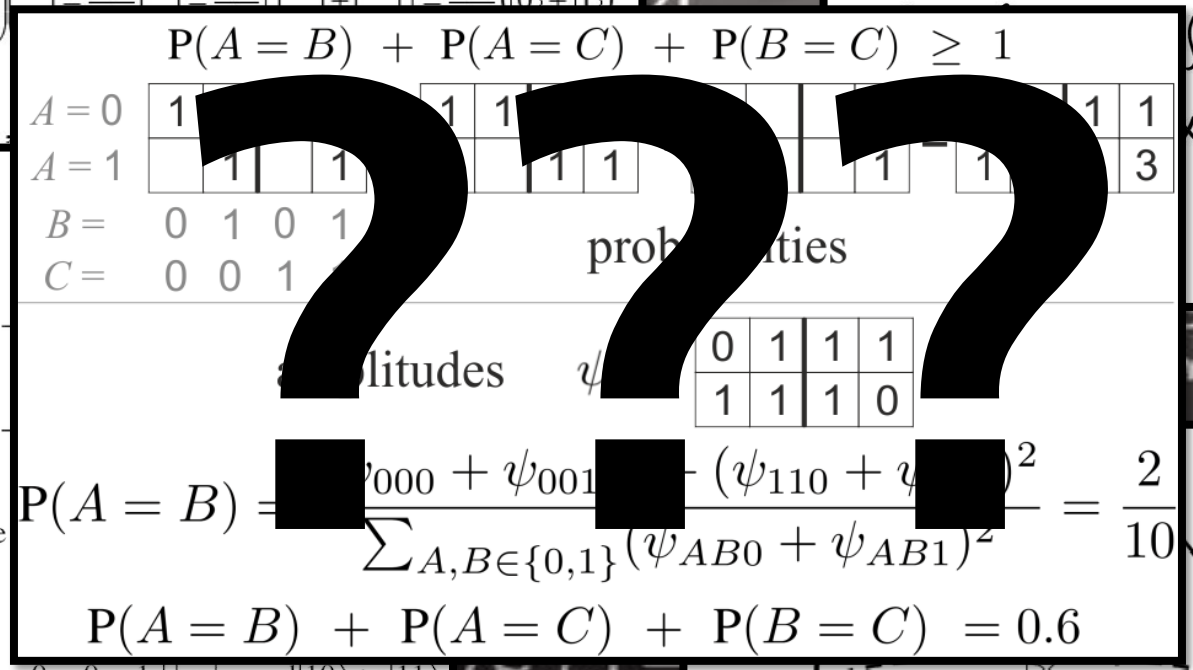
not yet usefull, **but HUGE potential !**

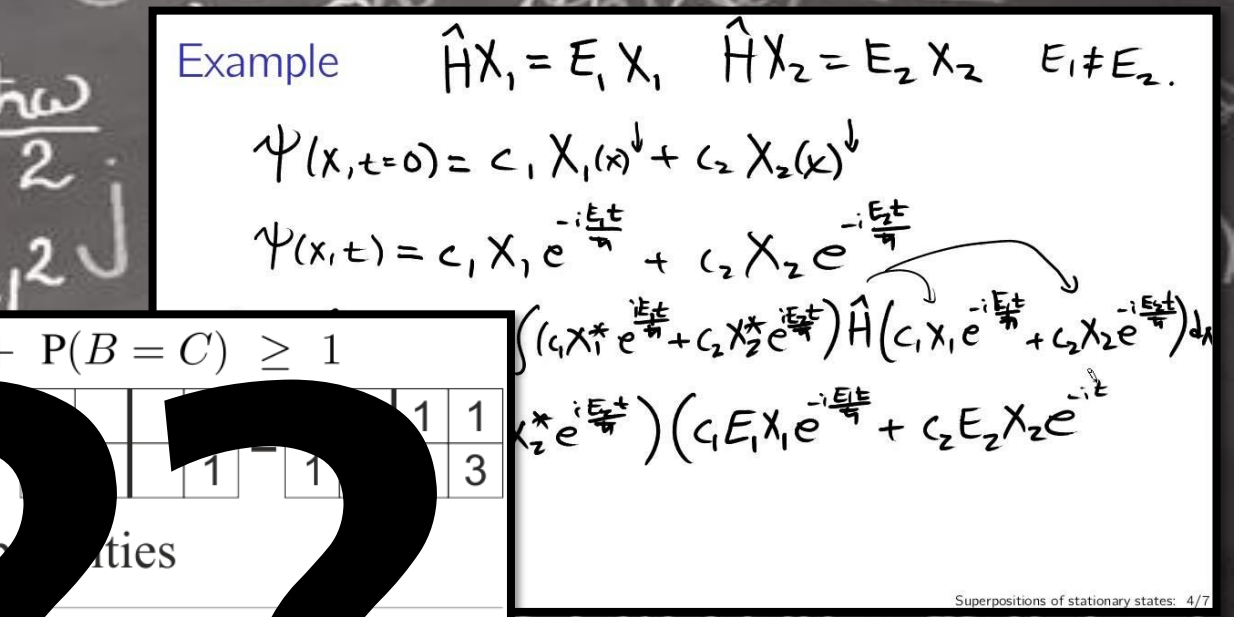
(for specific problems)
Simulation, optimization, machine learning, finance…

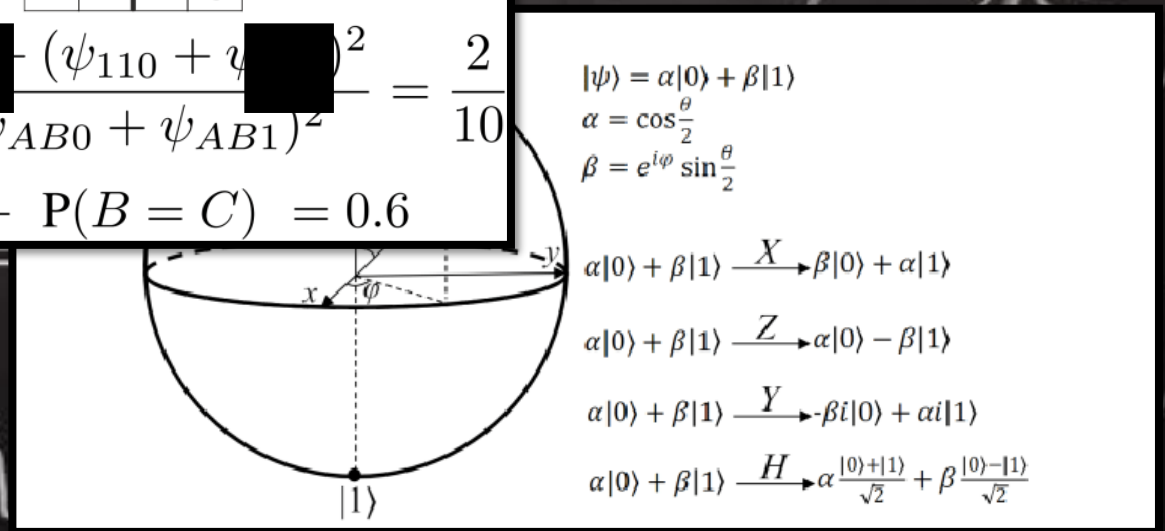
Quantum Computing ??



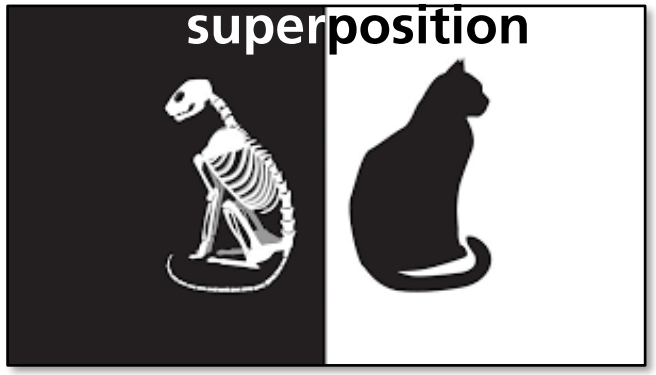






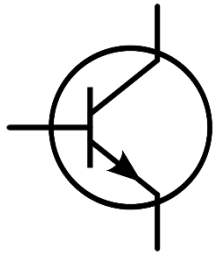


Quantum Computing ?

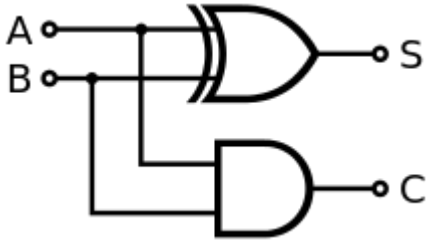


Quantum Computing (!)

classical



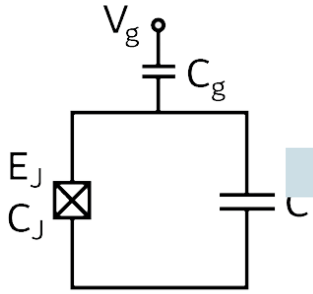
Transistor → Bit



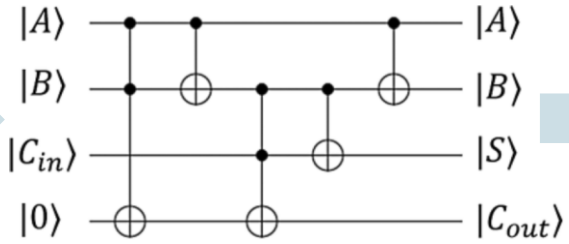
classical half adder

Integrated circuits

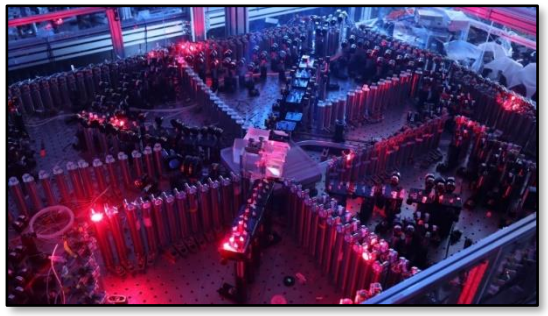
quantum



Transmon → QuBit



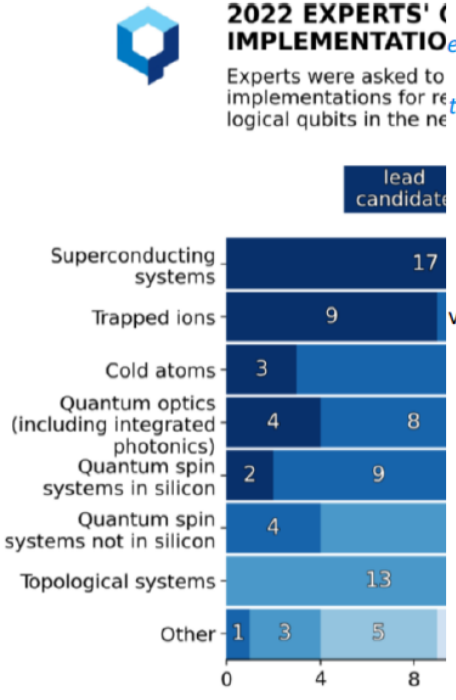
adder with quantum gates



Photonic quantum system

State of Play

The Qubit level: different platforms



	atoms		electron superconducting loops & controlled spin				photons
qubit type	**trapped ions**	**cold atoms**	**super-conducting**	**silicon**	**NV centers**	**Majorana fermions**	**photons**
cryogeny	<300W	N/A	16 kW				
vacuum pumps[1]	vacuum	ultra-vacuum 100W	vacuum				
qubits gate controls	<1.4 kW ions heating, lasers, micro-aves generation, CMOS readout electronics	5,8 kW atoms heater, lasers, control (SLM, etc) and readout image sensor + electronics	from 20 mW depending on micro-wave ge inside t				
computing	1 kW	1 kW	1 kW	1 kW	<1 KW	1 KW	700 W
# qubits used	24	100-1000	53-433	4-15	N/A	N/A	20
total	**2 kW** (4)	**7-20 kW** (1)	**26 kW** (2)	**21 kW**	**N/A**	**N/A**	**4 kW** (3)

[1] : fixed energetic cost, for preping stage

typical configurations for Pasqal (1), Google Sycamore with 53 qubits (2), Quandela/QuiX (3), AQT (4) rough estimates for others

Table CEQIP-23 Gate-Based Quantum Computing Status Summary

Qubit type	*Quantum volume, (circuit size)*	*Qubit count*	*Qubit connectivity*	*2-qubit gate depth*	*Quantum teleportation*	*Qubit function*	*System scalability*
Superconducting	512 (9×9)	127	3.25	667	0.42 m	fair	fair
Trapped ion	4096 (10×10)	12	10	> 100 000	yes	fair	fair
Quantum dot	–	4	1	104	–	poor–fair	fair–good
Photonic	–	4			1400 km	poor	fair

2-qubit gate depth: ratio of coherence time divided by 2-qubit gate time (T_2^*/t_{2q})

Figure 18: quantum computing experts trust on
ions qubits. A few are trusting photonic and spi
Global Risk Institute [13].

Figure 30: existing QPU typical power drain and their source. Caveat: none of these systems provide a quantum advantage at this point in time (2023). Source: (cc) Olivier Ezratty, 2023.

Which Qubit platform „wins“ ?

Coherence time

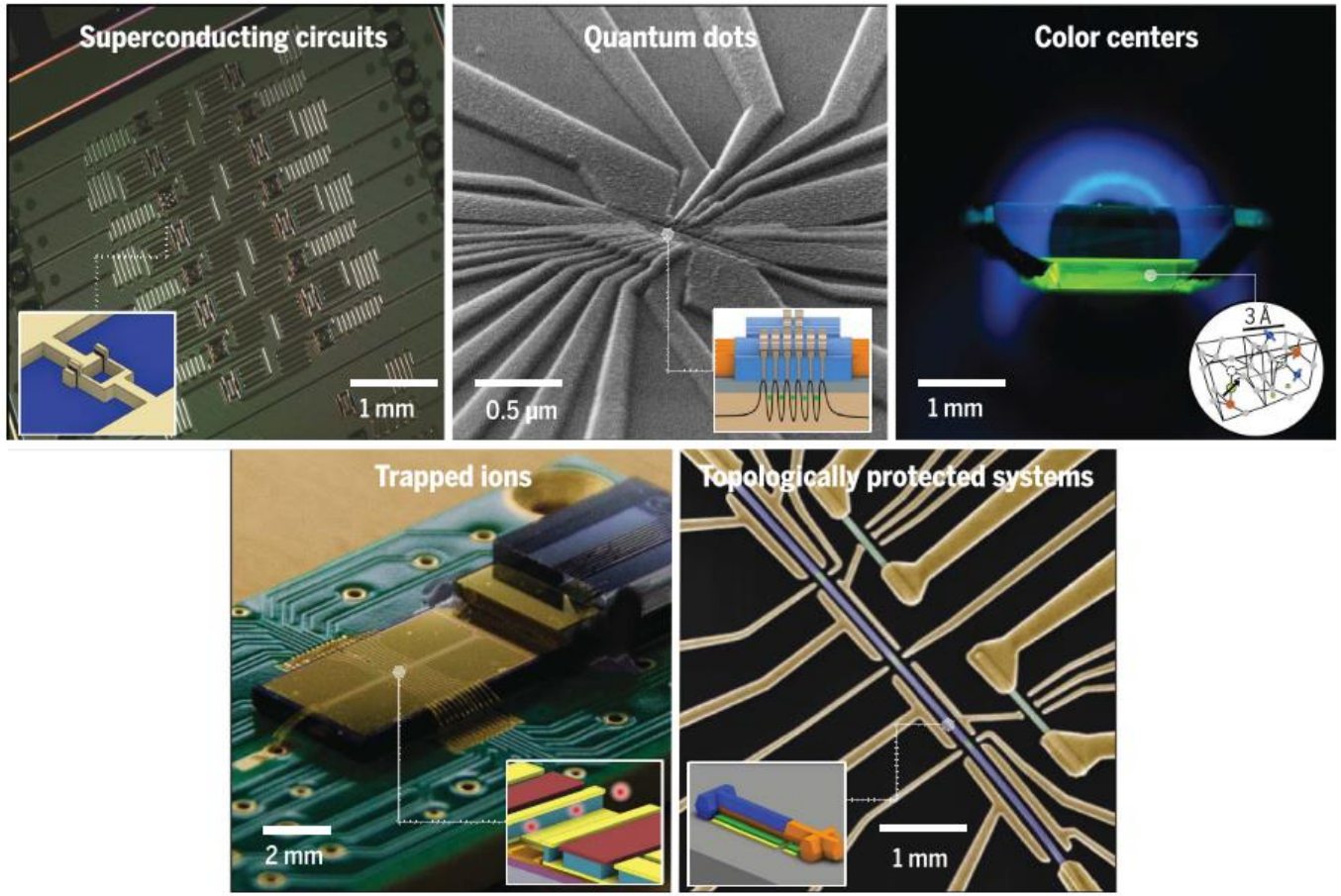
Fidelity

Ability to control

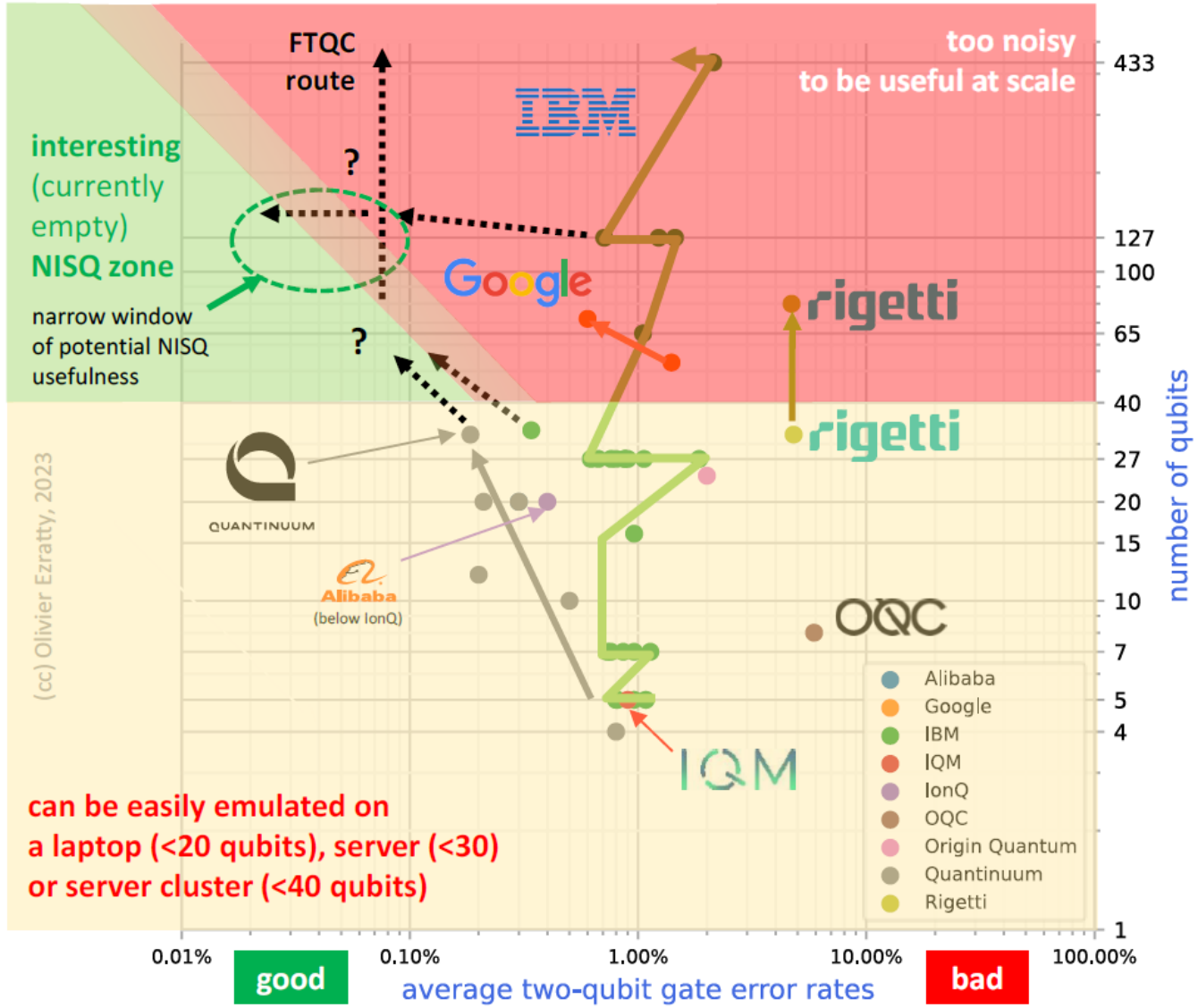
Scalebility

Ease of integration

…

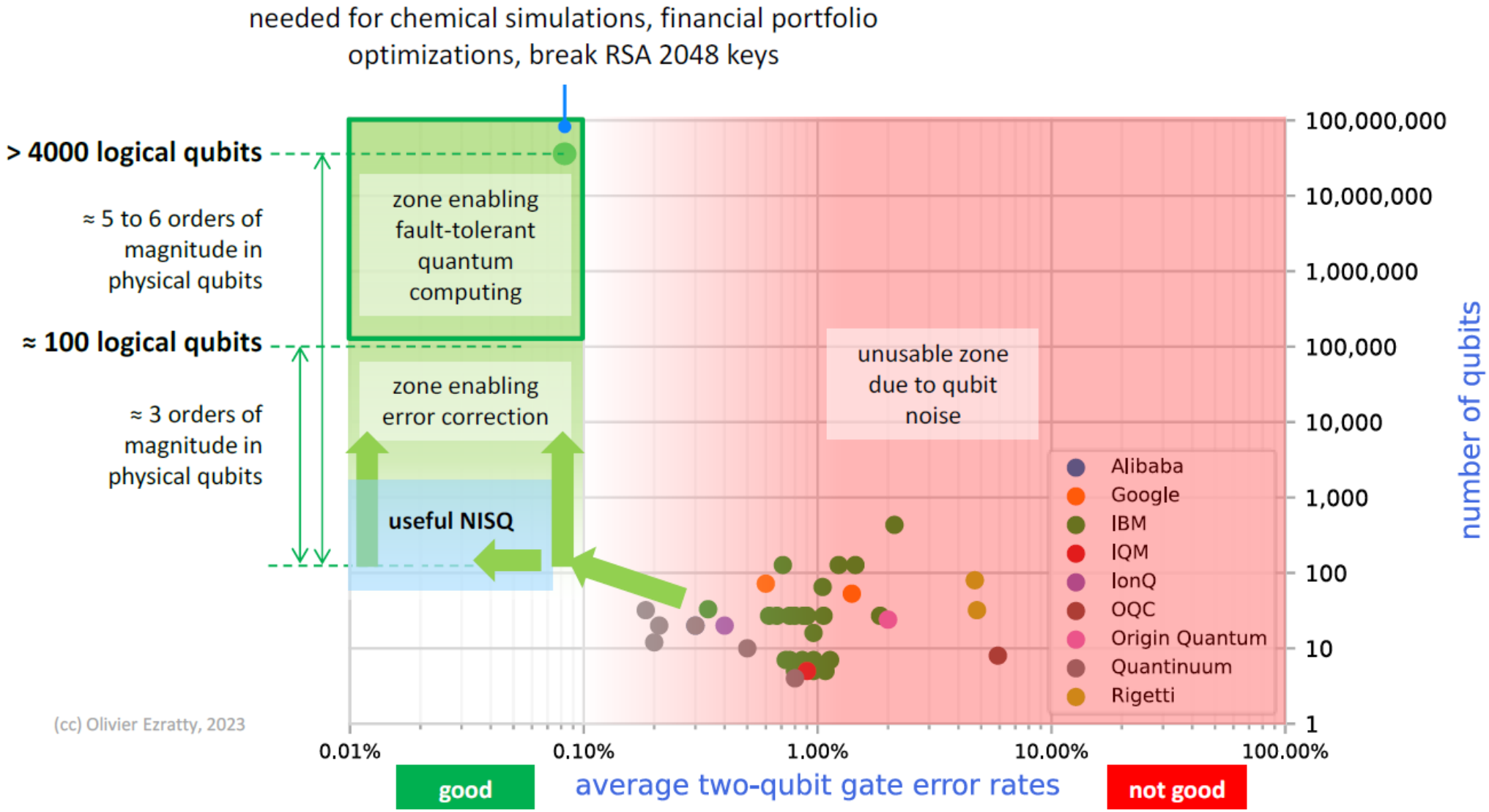


Current status for NISQ (more detailed)



Source: Olivier Ezratty, Kordzanganeh et al [10] and vendors two-qubit gate fidelities data obtained with randomized benchmarking

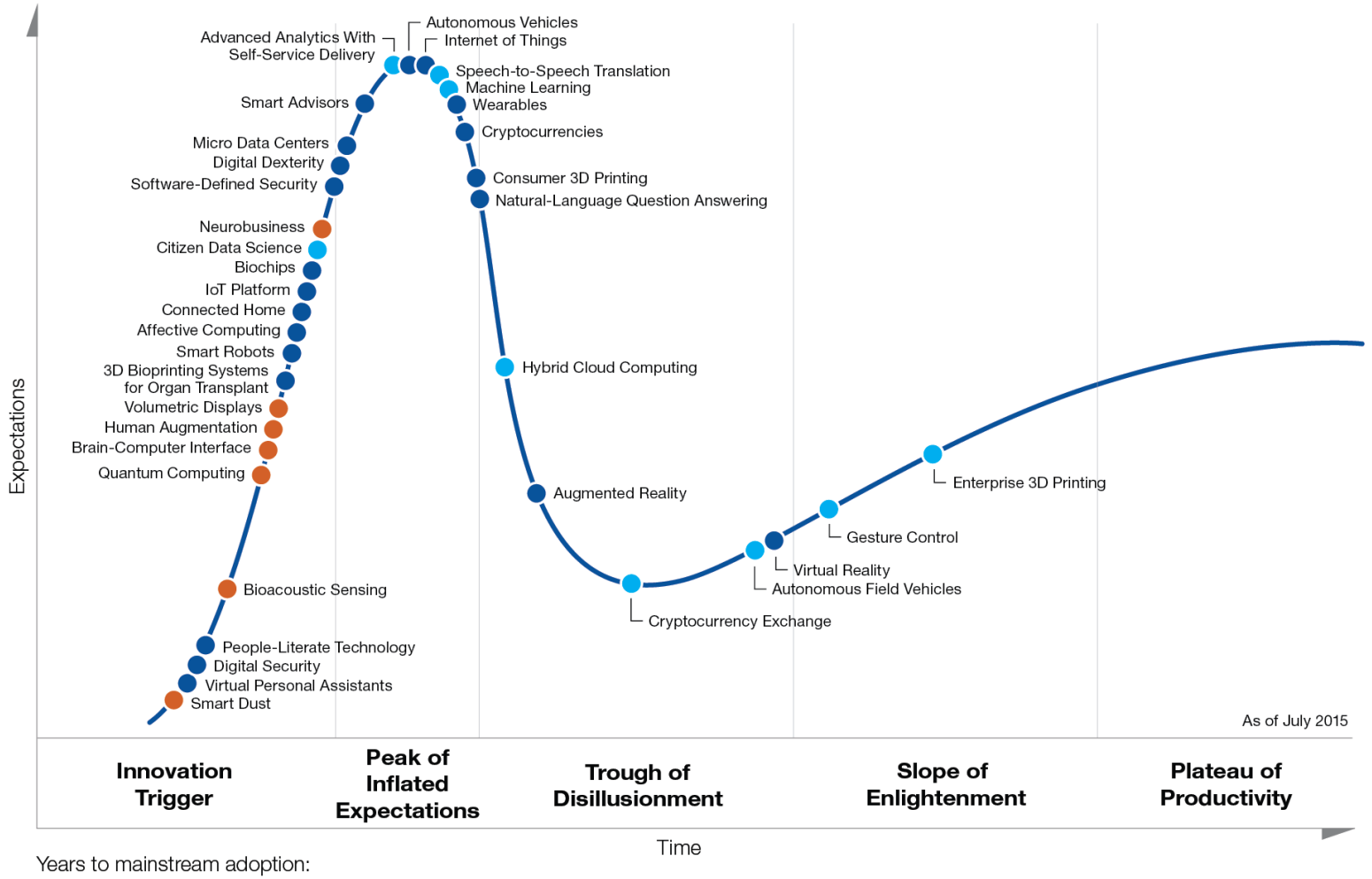
From NISQ to FTQC



Source: Olivier Ezratty, and vendor data, 2023

Quantum Computing in the Gartner Hypecycle

Emerging Technology Hype Cycle



Challenges and Microelectronics

Plenty of challenges

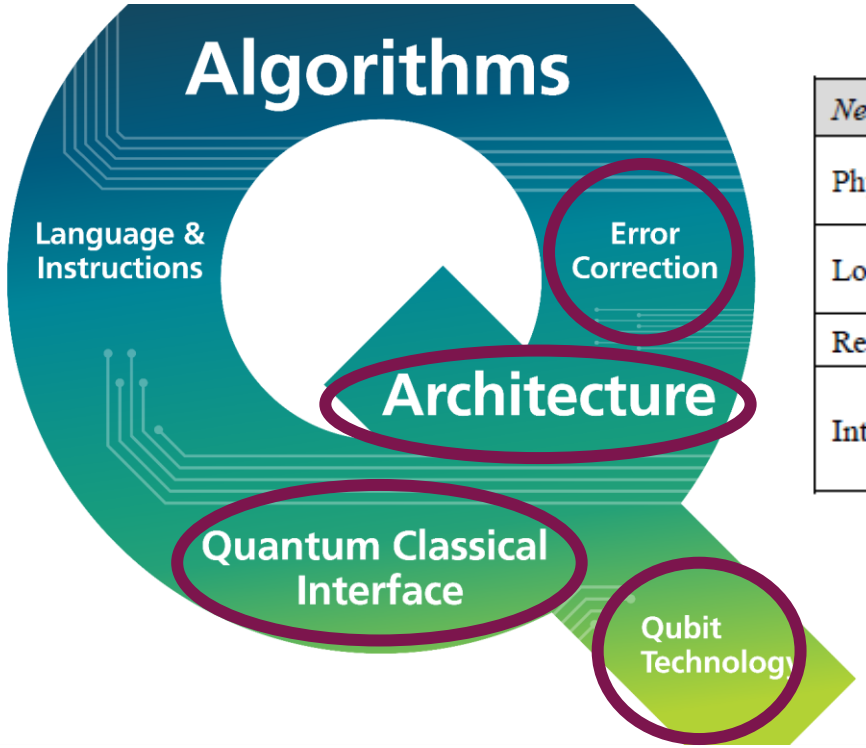
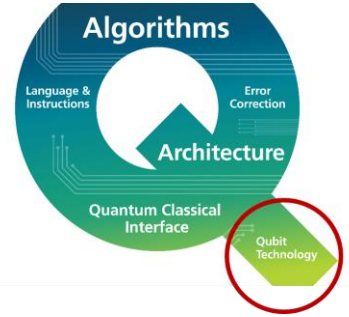


Table CEQIP-25 Difficult Challenges for QIP

Near-Term Challenges: 2022–2028	*Summary of Issues and Opportunities*
Physical qubits	Design and fabrication of qubit devices with enhanced qubit coherence times and gate fidelities
Logical qubits	Implementation of fully error-corrected logical qubits and protected gate operations
Readout of qubits	Development of scalable, cryogenic qubit readout hardware
Interconnects, cryogenic to room temperature	Development of low thermal conductance and high bandwidth interconnects between different temperature stages of cryogenic- and room-temperature electronics

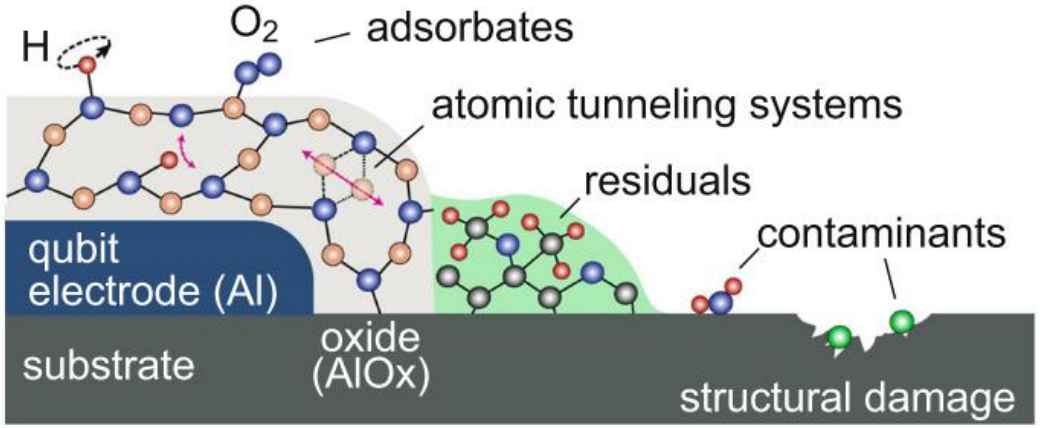
Challenges with Qubit Fabrication

e.g.for superconducting qubits

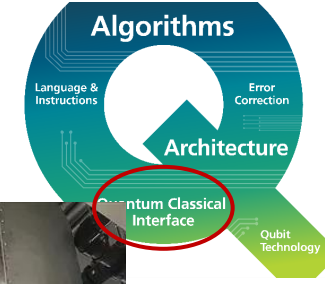


- Sensitivity to noise and losses
- Material and process imperfections
- Well defined, uniform and tight junction properties

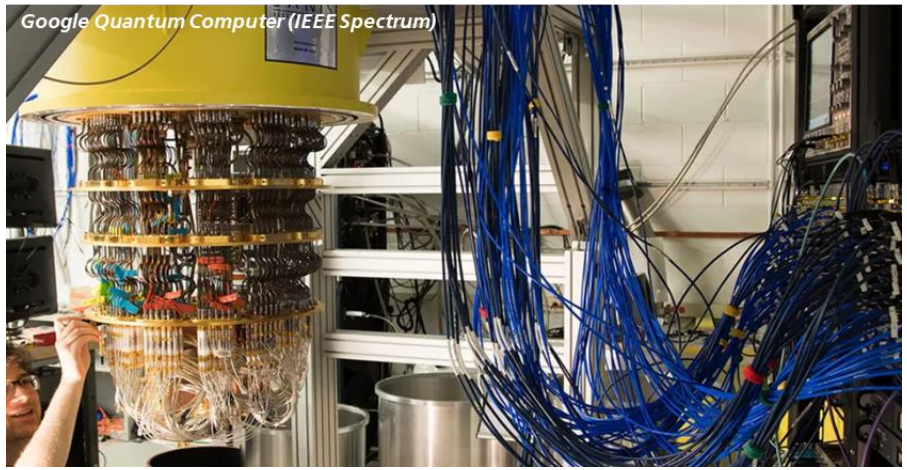
→ explore new material and better process capabilities, beyond the labs



Quantum-Classical Interface: the problem of Interconnects



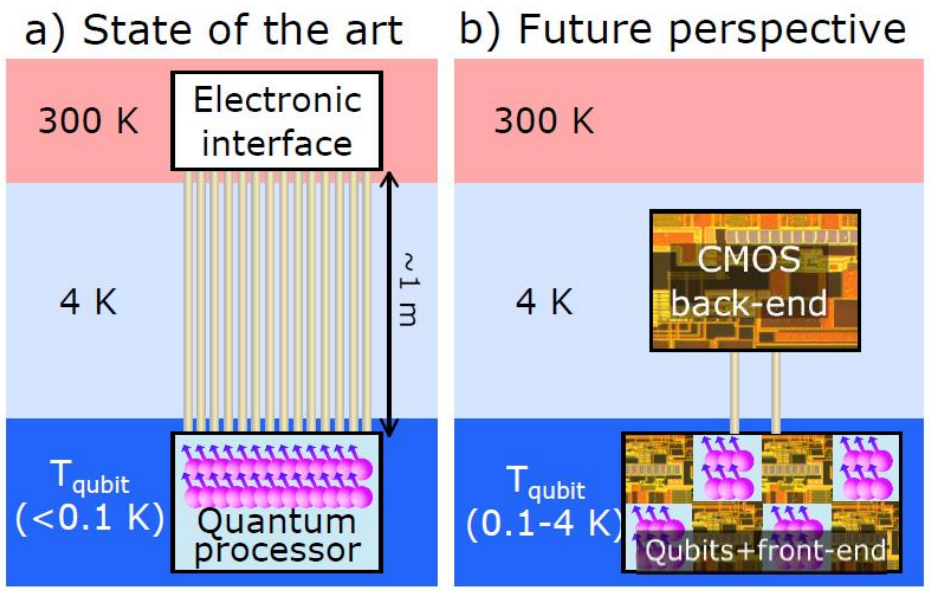
Incoming ‚wiring apocalypse'



?

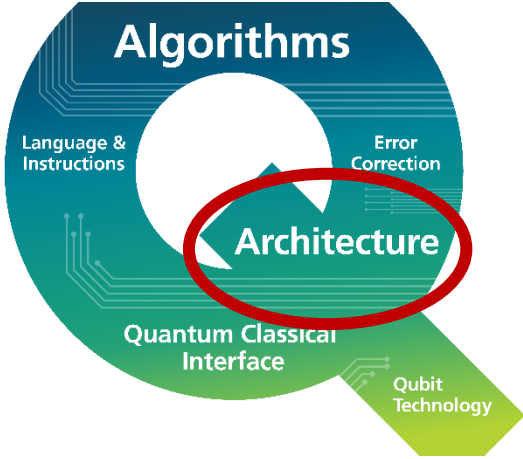
!

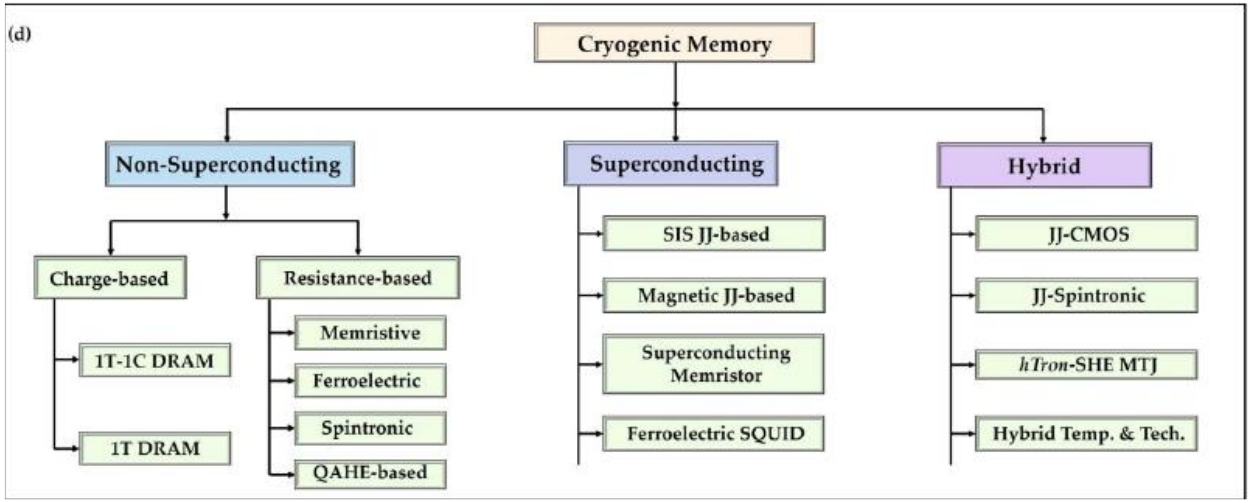
IBM



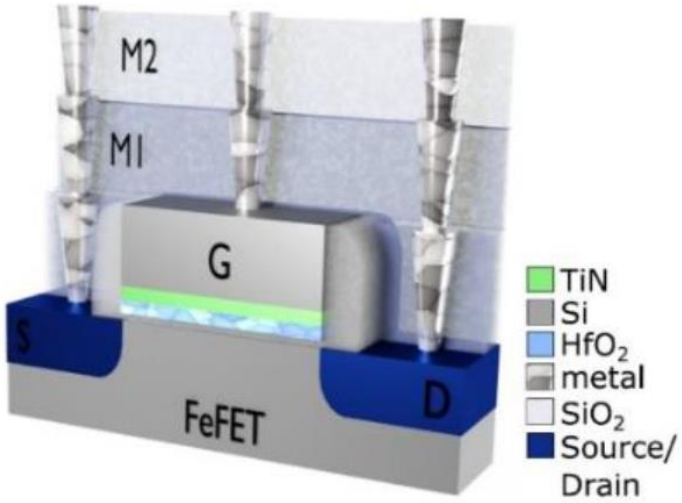
Dijk, J.P., Charbon, E., & Sebastiano, F. (2019). The electronic interface for quantum processors. Microsystems, 66, 90-101.

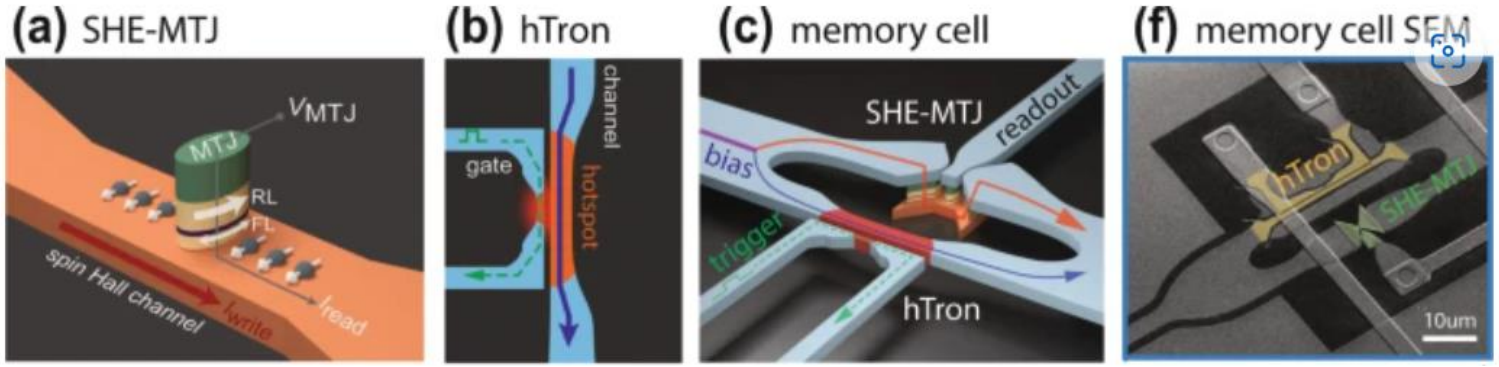
Quantum Memory





https://doi.org/10.48550/arXiv.2111.09436

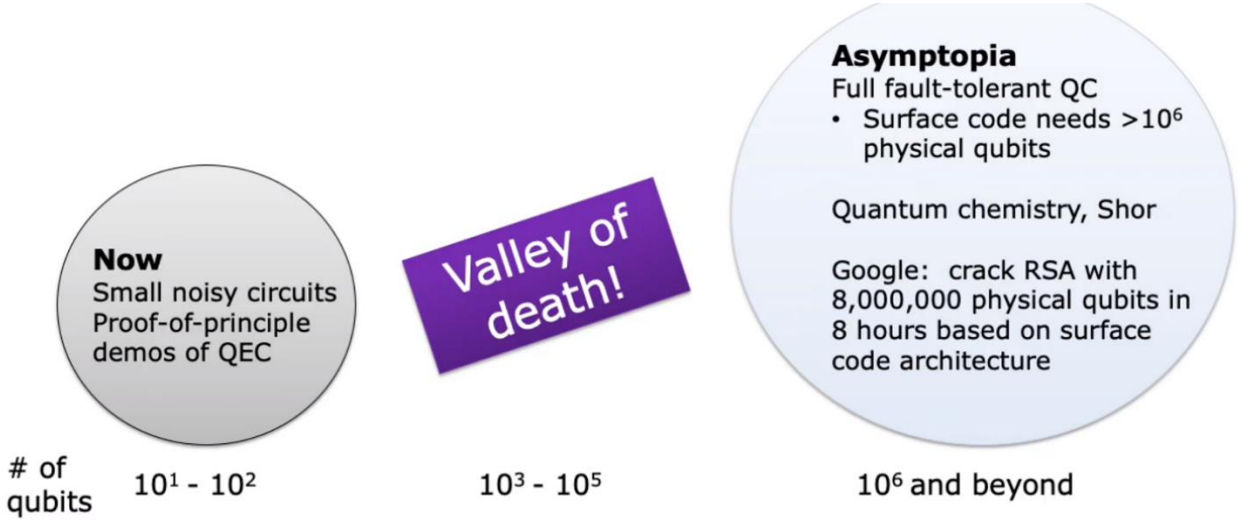




Do numbers matter?

Major qubit challenges:

- A) fidelity and coherence
- B) number



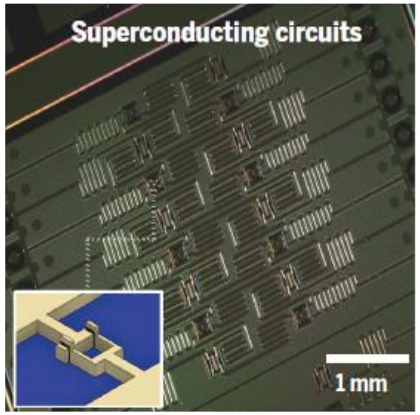
Quantum Motion

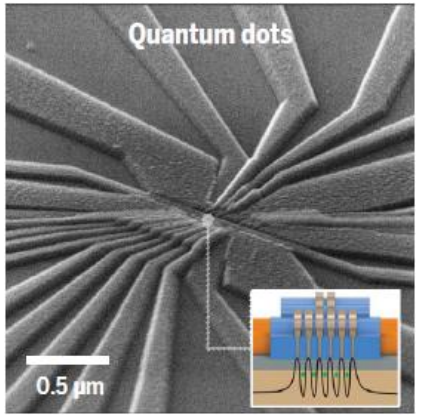
„Is there a technology that can reliably create billions of components on a chip and which is feasible for quantum computing?“

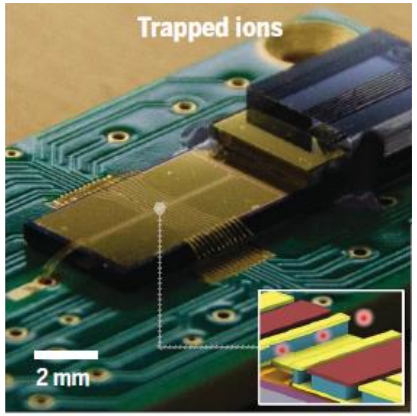
→ Microelectronics‘ Semiconductor manufacturing

Modern Semiconductor Manufacturing is needed for (large scale) Quantum Computing !

- **Number of qubits**
  - ❖ Error correction, size of quantum algorithms
- **Variability, process control and yield**
  - ❖ Improve qubit uniformity, coherence time and gate fidelity
- **Interconnects**
  - ❖ Spatial limitations, thermal budget, wiring ‚apocalypse'
- **Interface to classical electronics**
  - ❖ CMOS control electronics, Advanced packaging, variability control, FDSOI, …
- **Applicable to most platforms (SC, spin, ion trap, photonics, …)**
- **Relevant players also focusing on wafer level semiconductor manufacturing**
  - ❖ Intel, imec, CEA, PsiQuantum (with Globalfoundries), …







Paik et.al., Science 2021, Vol. 372, Issue 6539

Short interlude about Fraunhofer

Fraunhofer-Gesellschaft

At a Glance

- **Largest Organization for Applied Research in Europe**
- **Focusing on key future-relevant technologies**
- **Commercialization of findings in business and industry**

Joseph von Fraunhofer (1787-1826)

Scientist, inventor and entrepreneur

30,800 employees

76 institutes and research units

€ 3.0 billion total funding
€ 2.6 billion contract research

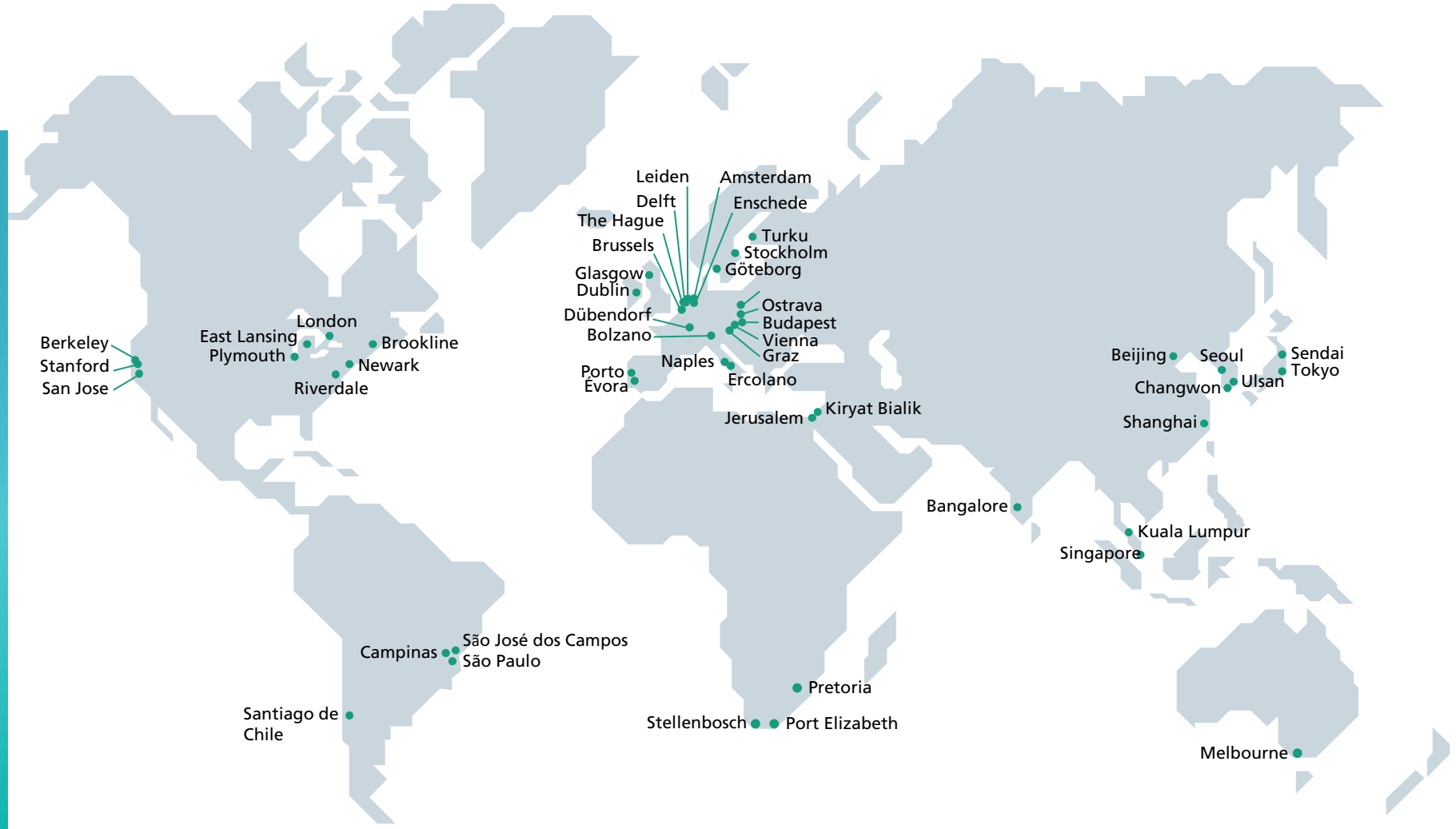
Base funding from Germany's federal and state governments

Industrial contracts and publicly-funded research projects

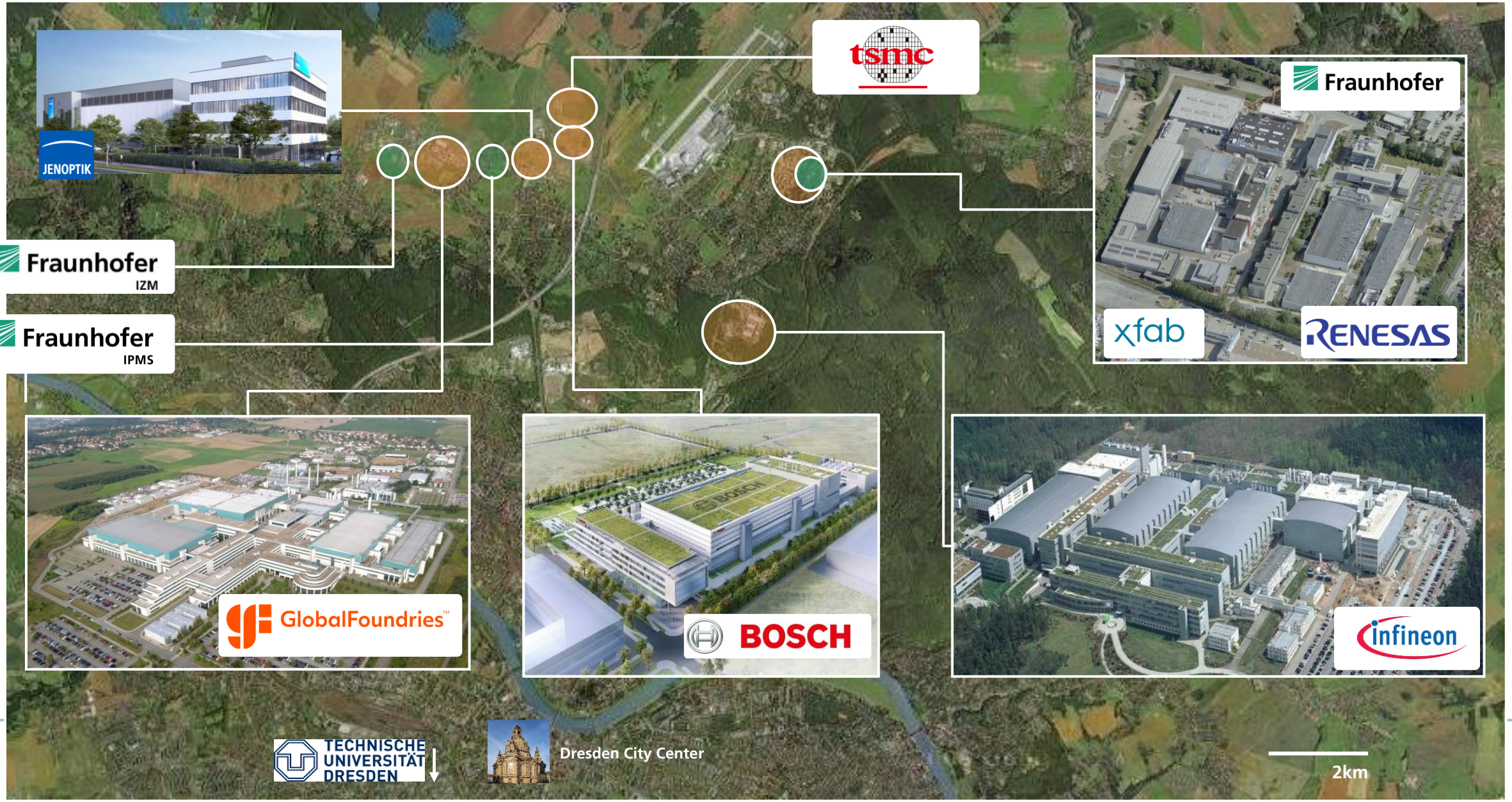
The Fraunhofer-Gesellschaft

International network

- **Eight independent international Fraunhofer affiliates**
- **Activities with partners in approximately 80 countries**
- **Representative offices and senior advisors around the world build bridges to local markets**



Silicon Saxony - The heart of European Microelectronics beats in Dresden



Fraunhofer IPMS

Headquarter Dresden

At a Glance

- 565 employees
- € 56 M annual revenue
- € 26 M industry contracts (thereof)

R&D Focus:

- Photonic microsystems (200mm)
- Micro- and Nanoelectronic technologies (300mm)

Fraunhofer IPMS – Center Nanoelectronic Technologies (CNT)

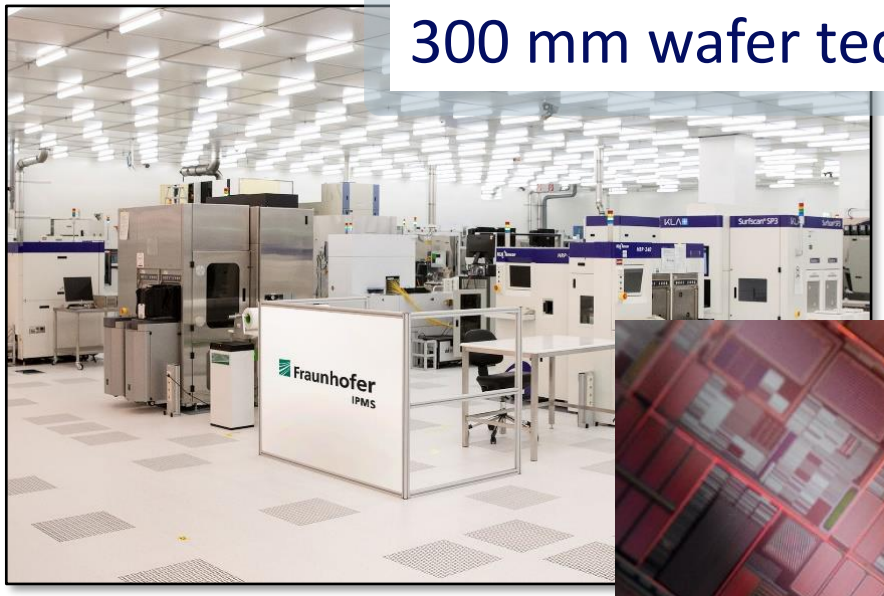
IPMS-CNT's research focus:

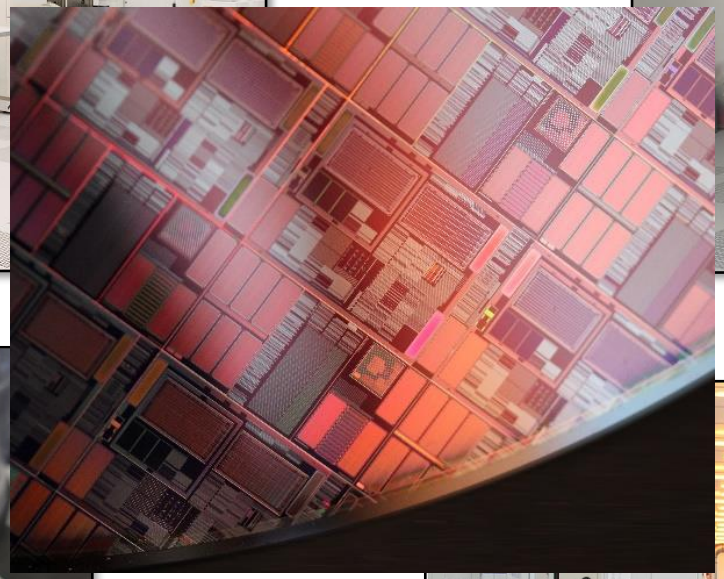
- **Non-Volatile Memories** (NVM)
- **Screening Fab Services** incl. process development in Back-End-of-Line module
- **AI Fab** with focus on Edge AI System Integration and **Compute-In-Memory** concepts
- **Quantum Computing**

FhG-IPMS capabilities for QC

300 mm wafer technologies & Cryo-characterization

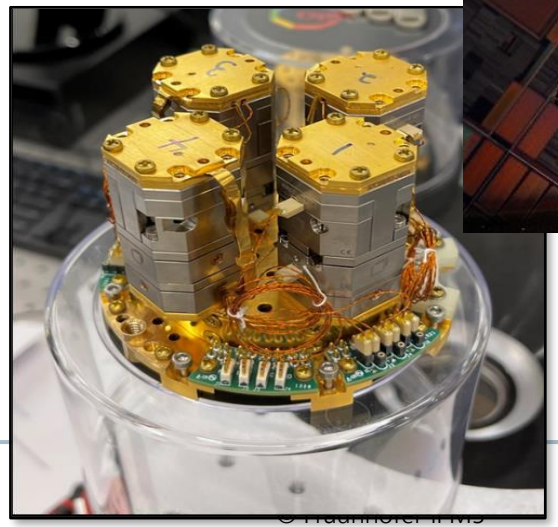
300mm cleanroom at CNT





300 mm UHV cluster PVD

Cryo Characterization

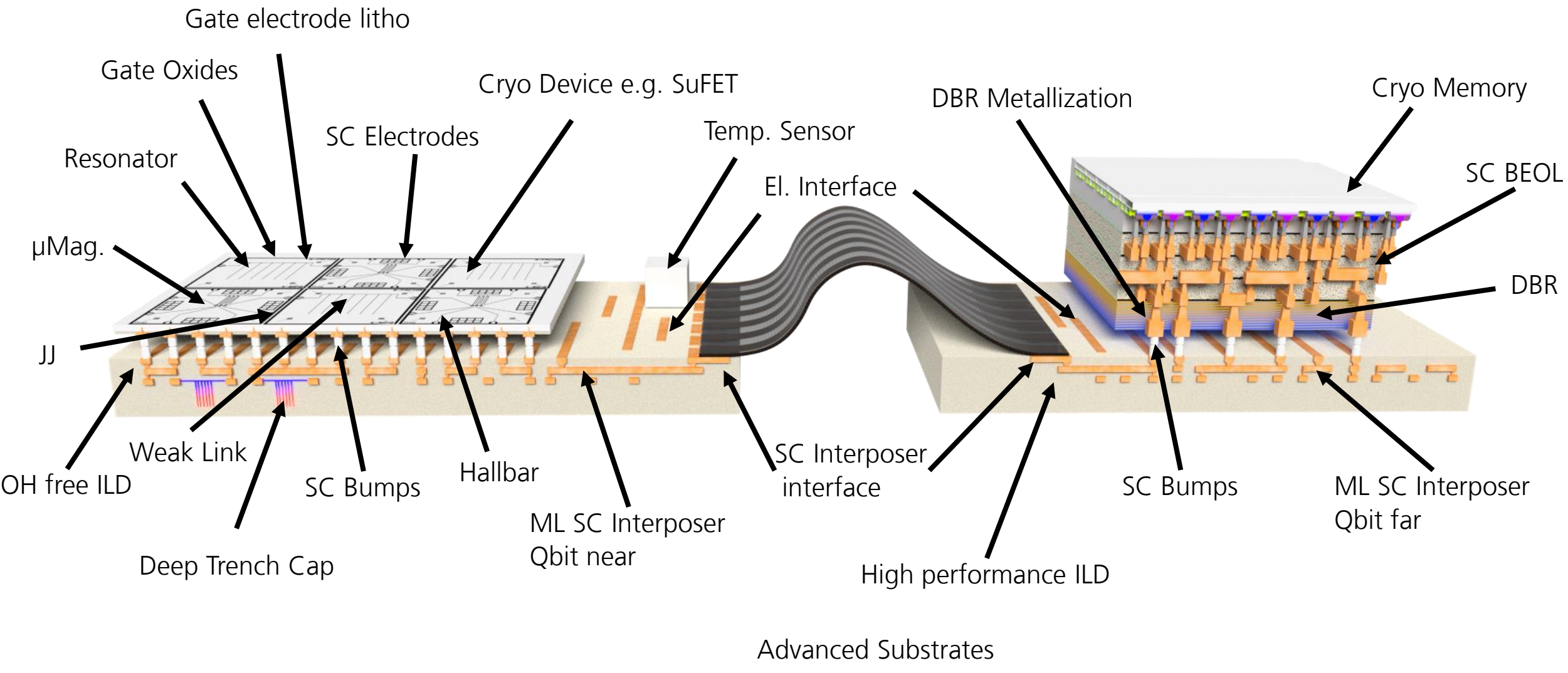


300mm cleanroom at CNT

Solutions (or at least ideas !)
with a few examples

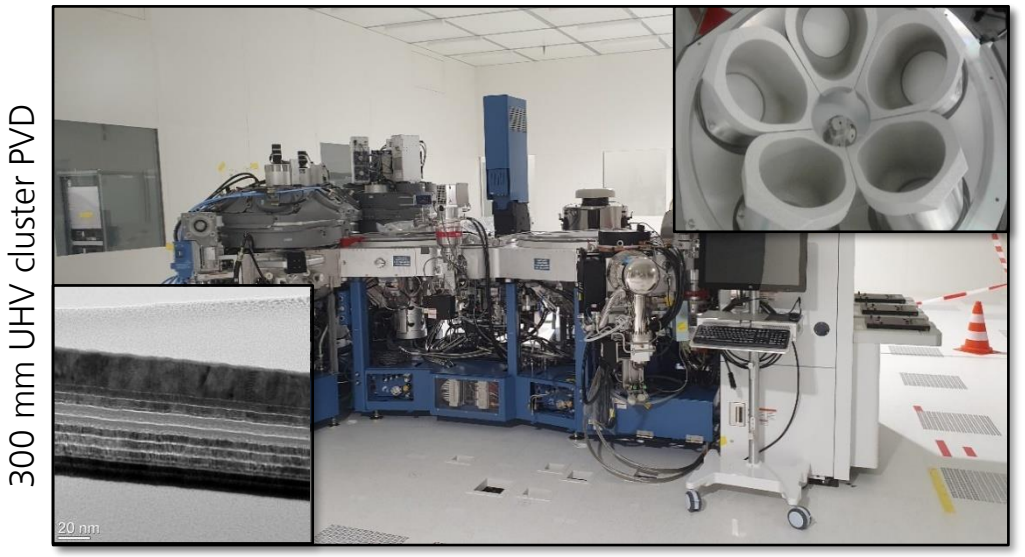
Building blocks for integrated QC-systems

Neuromophic Error Correction



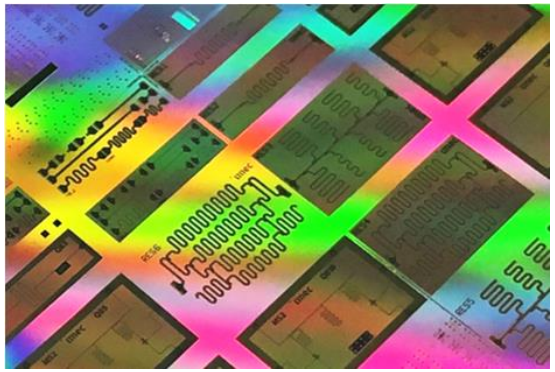
Current project engagement for Superconducting Qubits

- QSOLID project (FZ Jülich): build a large scale German quantum computer
- MATQ project: Set up European supply chain and eco system for superconducting QC
- Task IPMS:
  Multi target PVD for superconducting devices and qubits, resonator fabrication, packaging solutions, cryo characterization
- Engagement in QuPilot project for superconducting platform



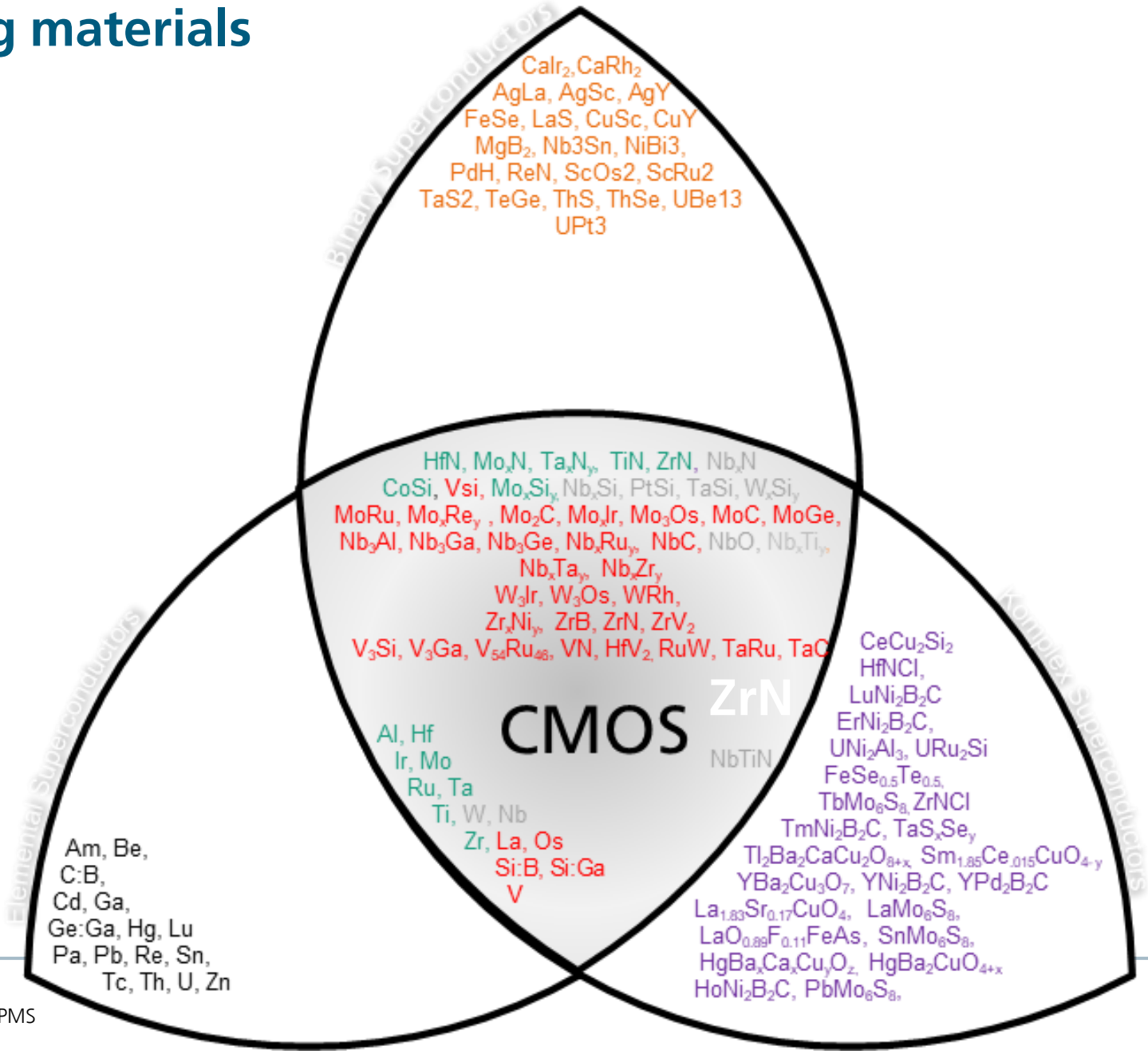
300 mm UHV cluster PVD

300mm cleanroom at CNT



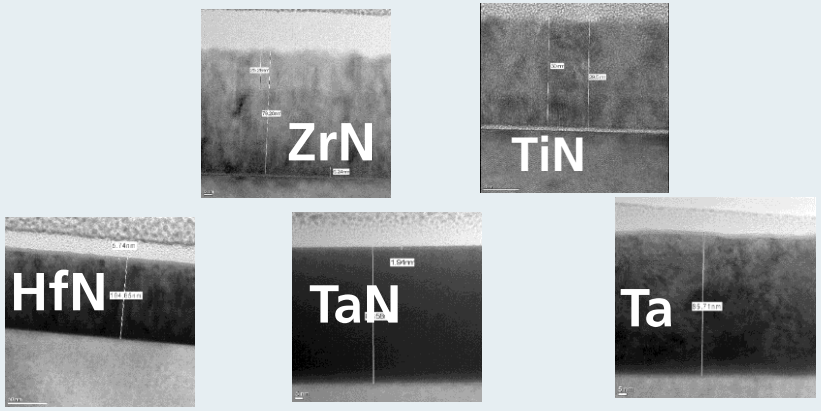
Imec SC testchip

New superconducting materials

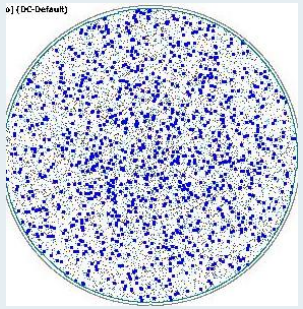


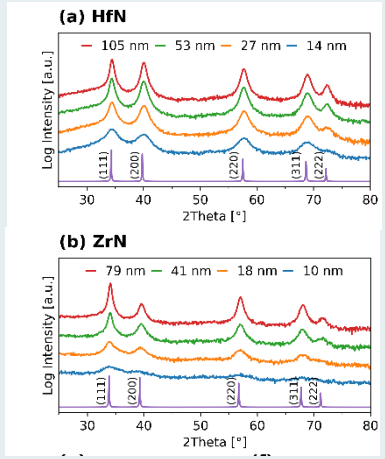
Research on new SC materials

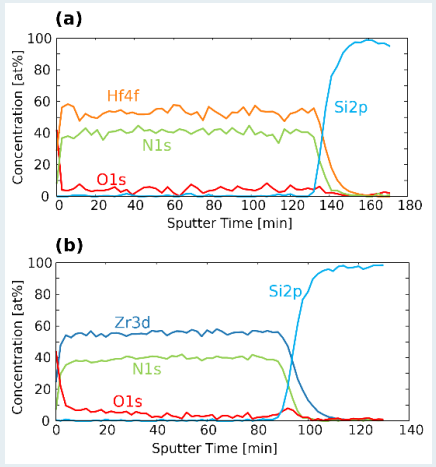
Deposition



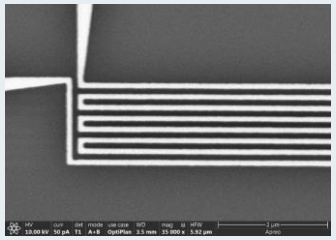
Metrology and Analytics

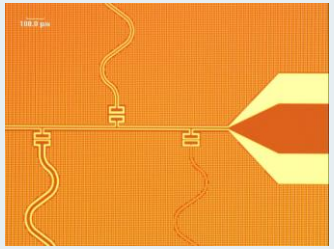






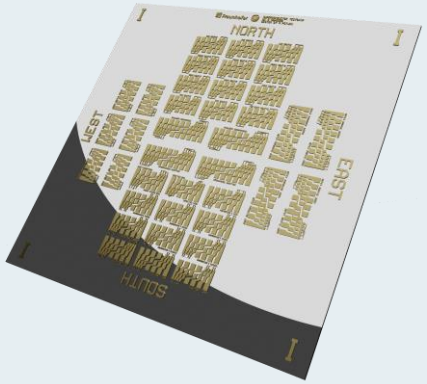
Patterning





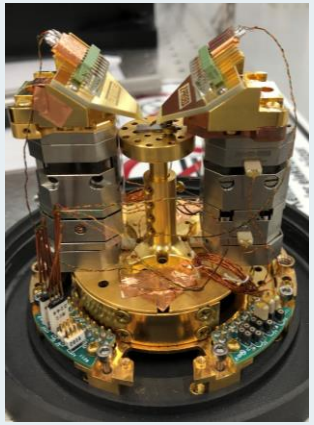
ZrN serpentines

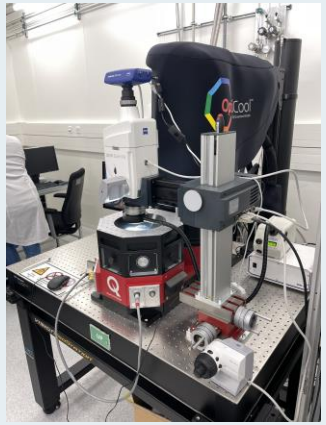
Resonator fabrication

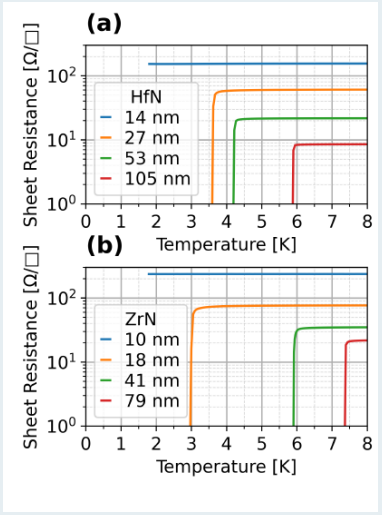


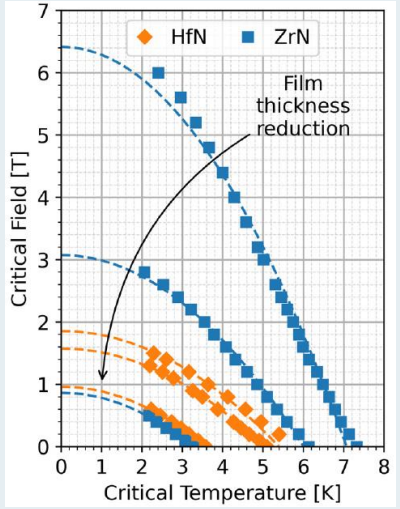
Testchip

Cryo setup and characterization







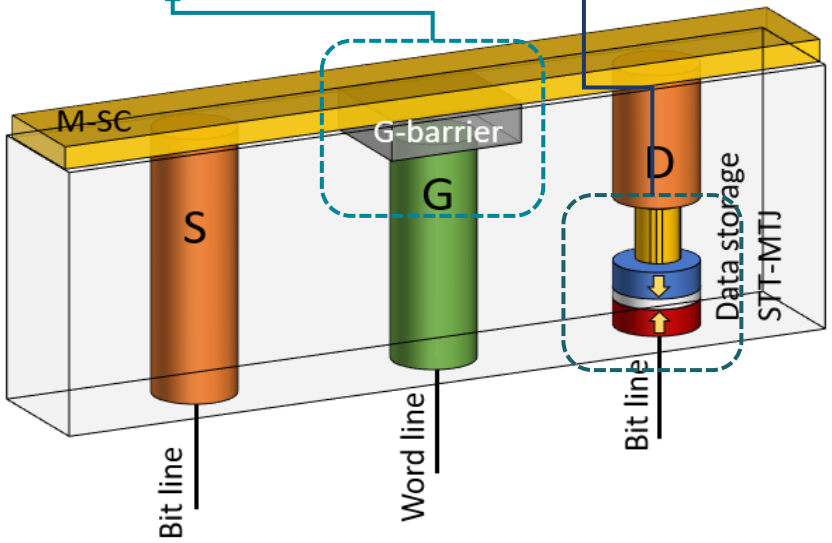


CONDOR concept

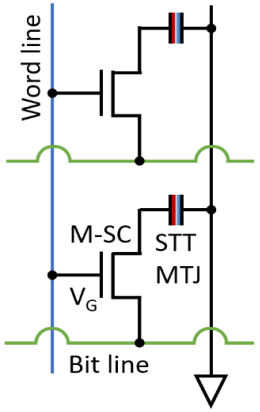
Superconducting spintronic devices for cryogenic electronics

Gate controlled superconductivity

Cryogenic memory



- Ultra low power
- Fast switching
- CMOS integration



MAX PLANCK INSTITUTE OF MICROSTRUCTURE PHYSICS

Fraunhofer IPMS

Applications

- Quantum Computing
- Space
- Power Grid

37

Silicon spin qubits

QUASAR

- **German 200/300mm QPU line**

JÜLICH Forschungszentrum · ihp · Fraunhofer · Infineon

- Task IPMS:
  Nanopatterning for q-dots and shuttling concepts, integrated micro magnets and gate dielectrics

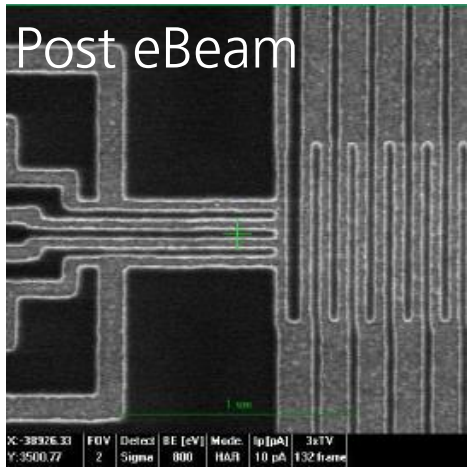
- **300mm Pilot Line for Quantum Computing** (Qu-Pilot project)

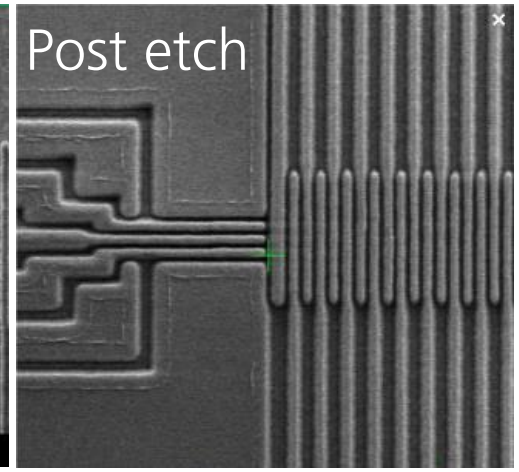
- Developing superconducting BEOL with CMOS compatible materials

leti ceatech · imec

QU-TEST & QU-PILOT

fine pitch gate patterning

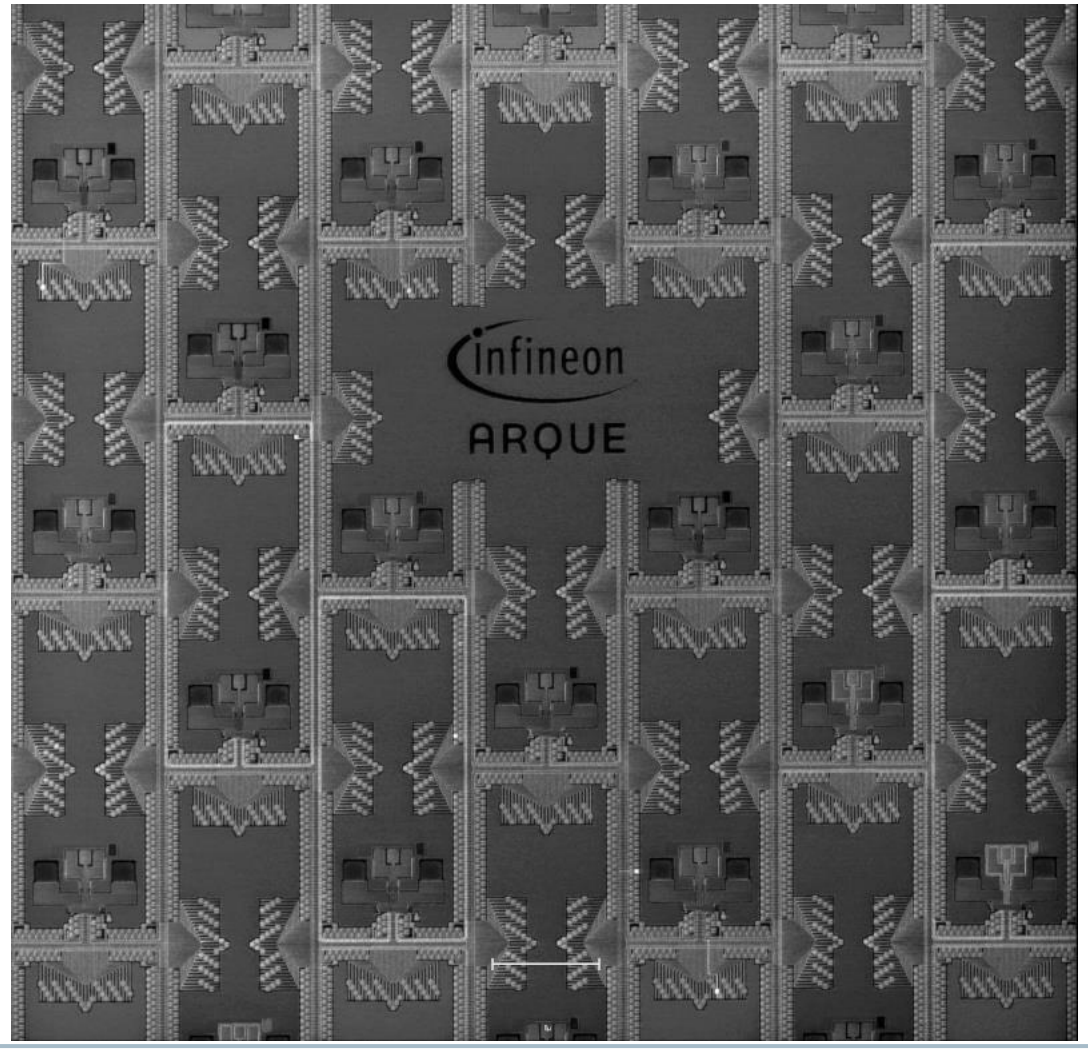




300mm cleanroom at CNT

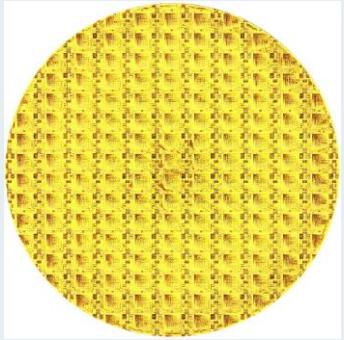
High resolution patterning studies

- eBeam with positive CAR reaching down to 20nm CD
- Stitching possible with <10nm missmatch
- 193nm Litho to eBeam alignment ~ 30nm
- Use in silicon spin qubit manufacturing route with partners



Integration of micro magnets

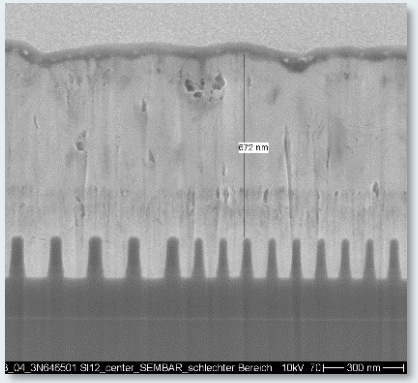
Deposition of cobalt



ECD

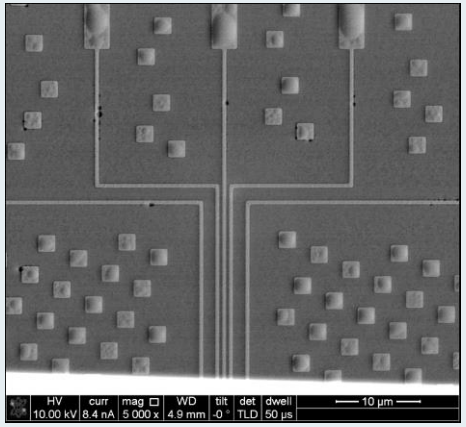
PVD (AMAT "Clover" Endura II)

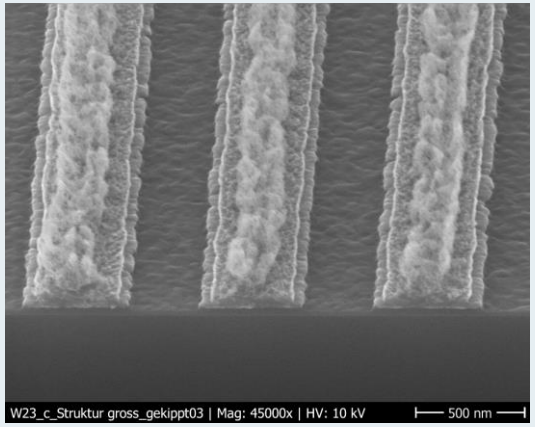
MOCVD (AMAT „Volta")



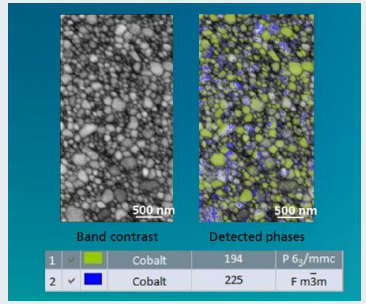
SEM X-section of Co filled trenches

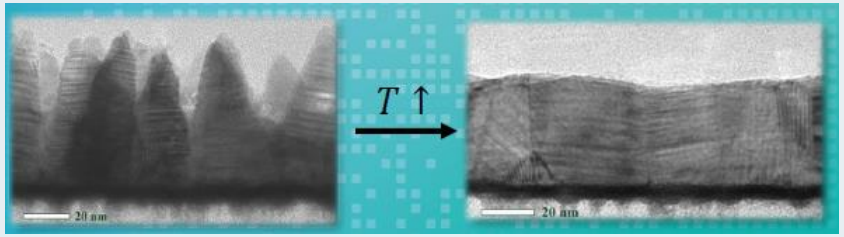
Patterning by RIE





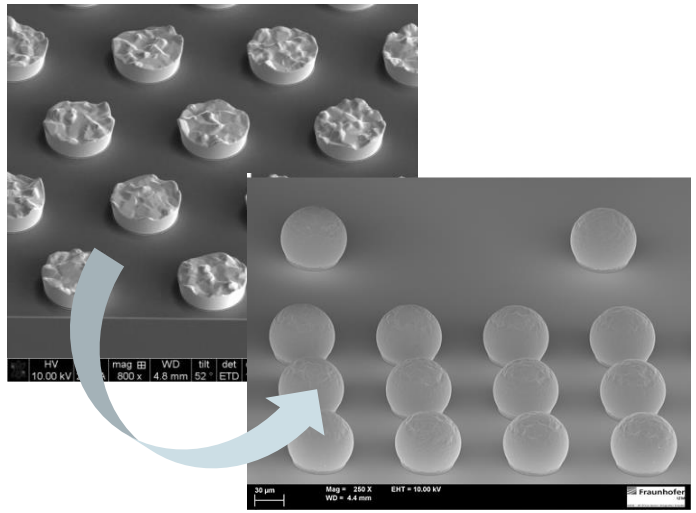
Metrology and Analytics





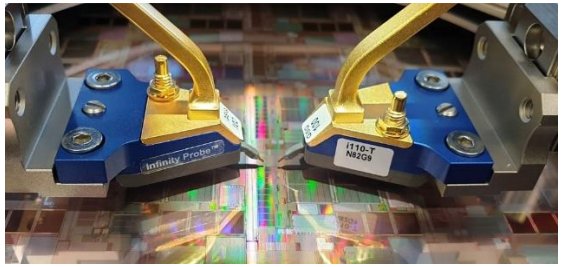
Further examples for modules which need to be looked at

Indium bumping for superconducting packaging options



Cryo chacterization of CMOS logic circuits for qubit control

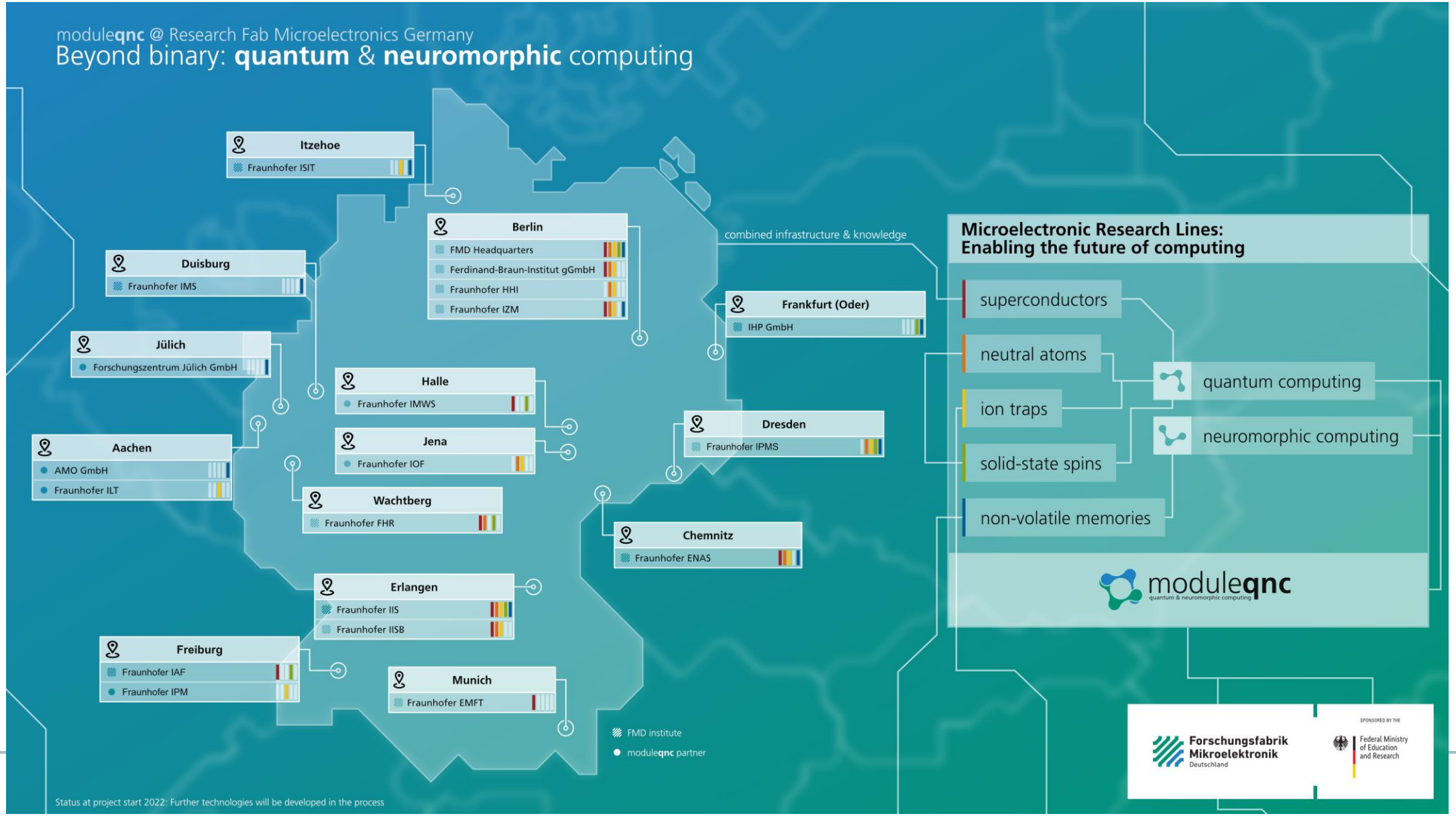
- E.g. FDSOI technology based



GlobalFoundries™

European strategy

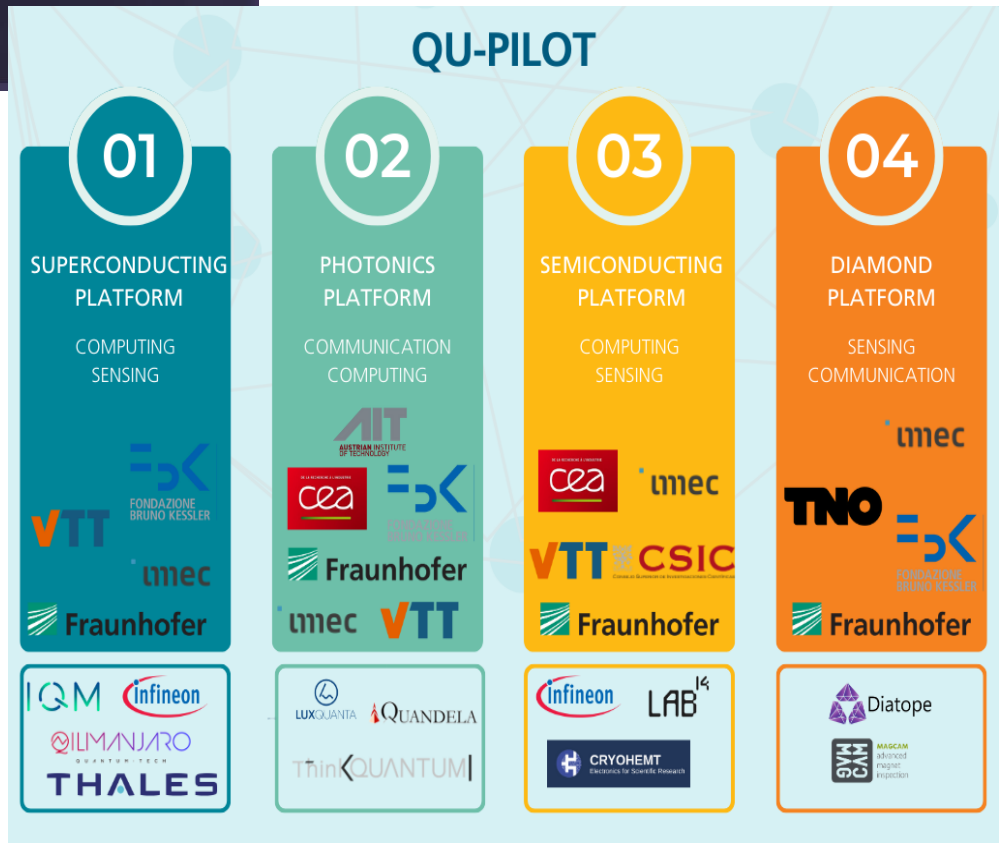
How to access those capabilities? Pilotlines !



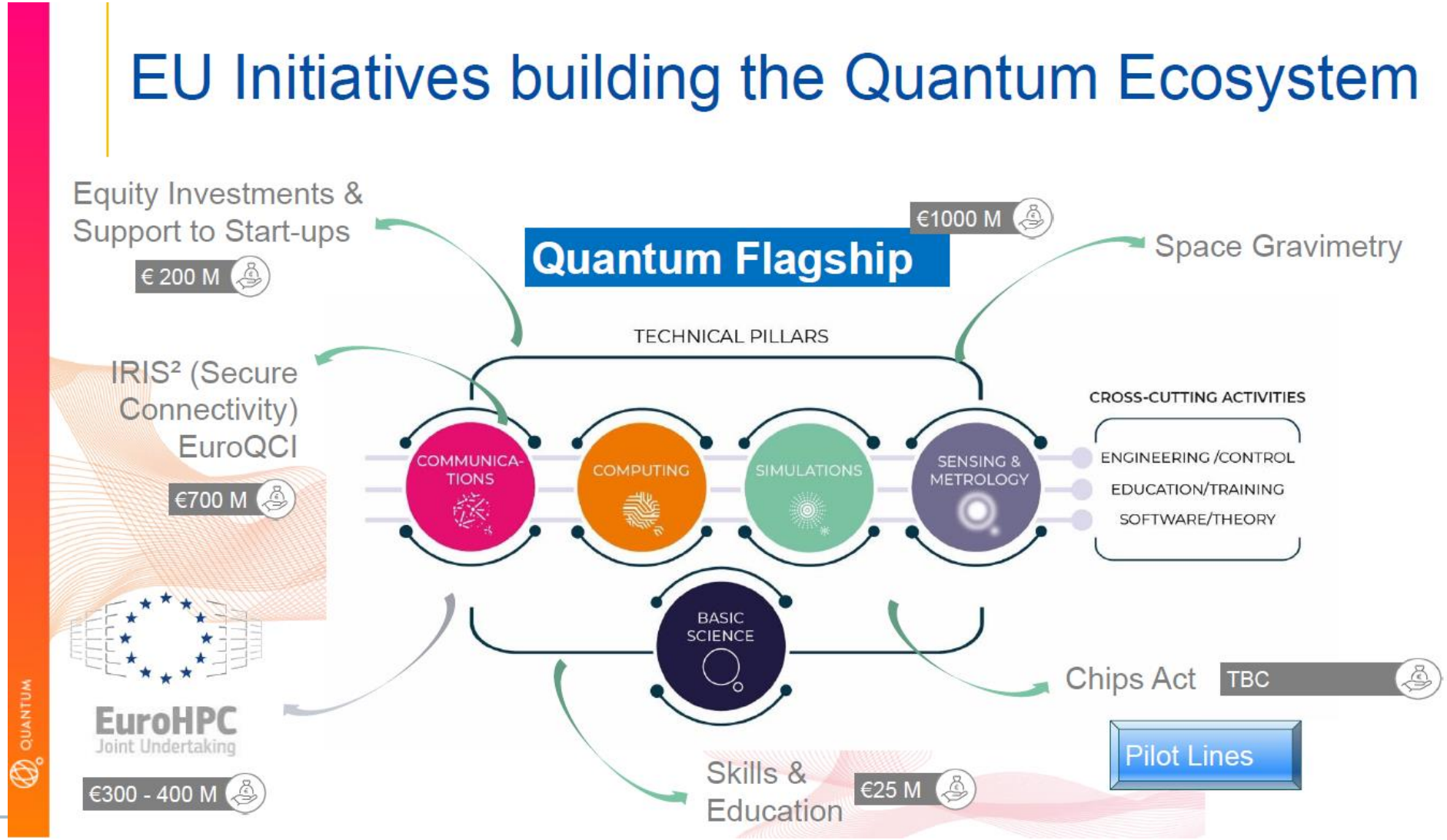
European programs Qu-Pilot & Qu-Test

HIGHLIGHTS

40 PARTNERS
10 COUNTRIES
23 USE CASES
OPEN CALL
BUDGET OF € 38 MILLIONS
ECOSYSTEM PLATFORM
PILOT PRODUCTION
TESTING & EXPERIMENTATION



Europeans Chips Act

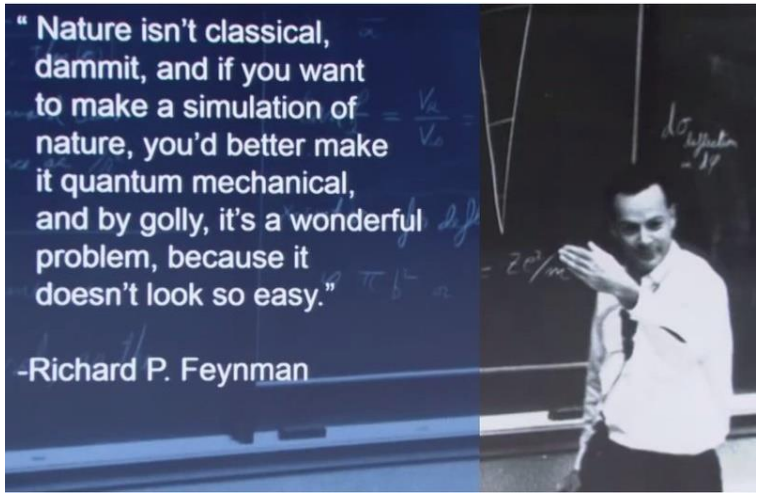


Summary quantum computing activities
USP of Fraunhofer IPMS QC

- Close collab with foundry and IDM nearby through established contamination and quality protocols, i.e. foundry- and IDM product wafers can be sent in and out of CNT without further checks !
- only semicon R&D site on 300mm in Germany, high visibility on national level
- close ties to IMEC; CEA-Leti and others
- Strategic commitment from Saxon government for further investments in Quantum Computing technology development towards large scaled systems
- We know how to enable great ideas and scale them on advanced wafer levels in close coop. with industry

Take Away Messages

- Quantum computation sounds weird, but that's just how nature is
- Real quantum advantage still 5-10 years away, currently might need millions of physical qbits



- On the road towards FTQC, quality **and** quantity needs to be improved
- For future larger scaled systems integration on chip/wafer level will be needed
- Microelectronics offers advantages for the whole quantum stack
- Cooperation is needed, key factor: the RTO pilotlines

Thank you, Questions?

Acknowledgement:
Roman Potjan (PhD student)
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Varvara Brackmann (senior researcher)