Innovations to Enable Future Logic Scaling

Sri Samavedam, SVP, CMOS Technologies
IMEC, Leuven, Belgium

Outline

- Historical Perspective
- Advanced Patterning
- New Device Architectures
- BEOL Evolution
- System Technology Co-optimization
- Environmental Impact of Logic Scaling

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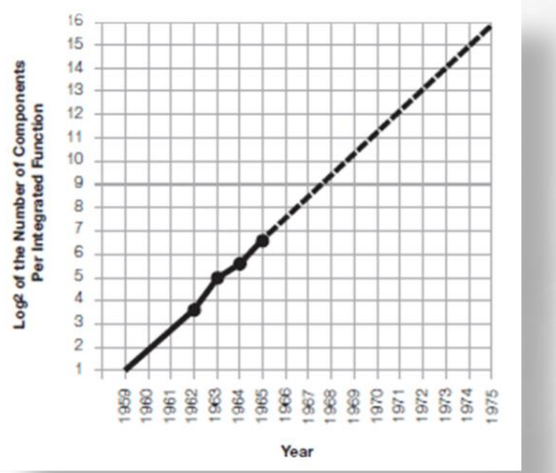
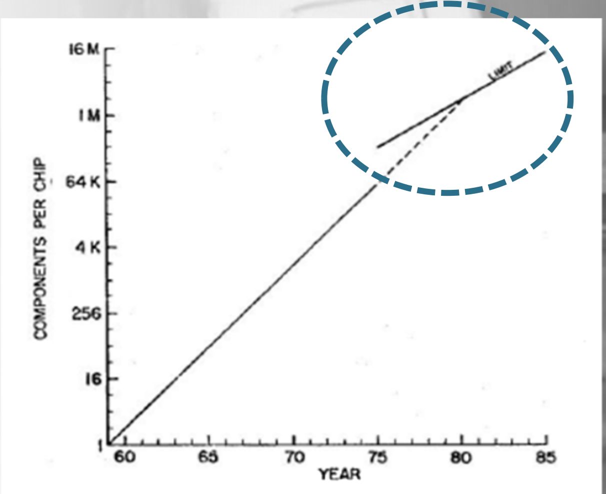
Gordon Moore's Predictions



1965: # of transistors in an IC double **every year**

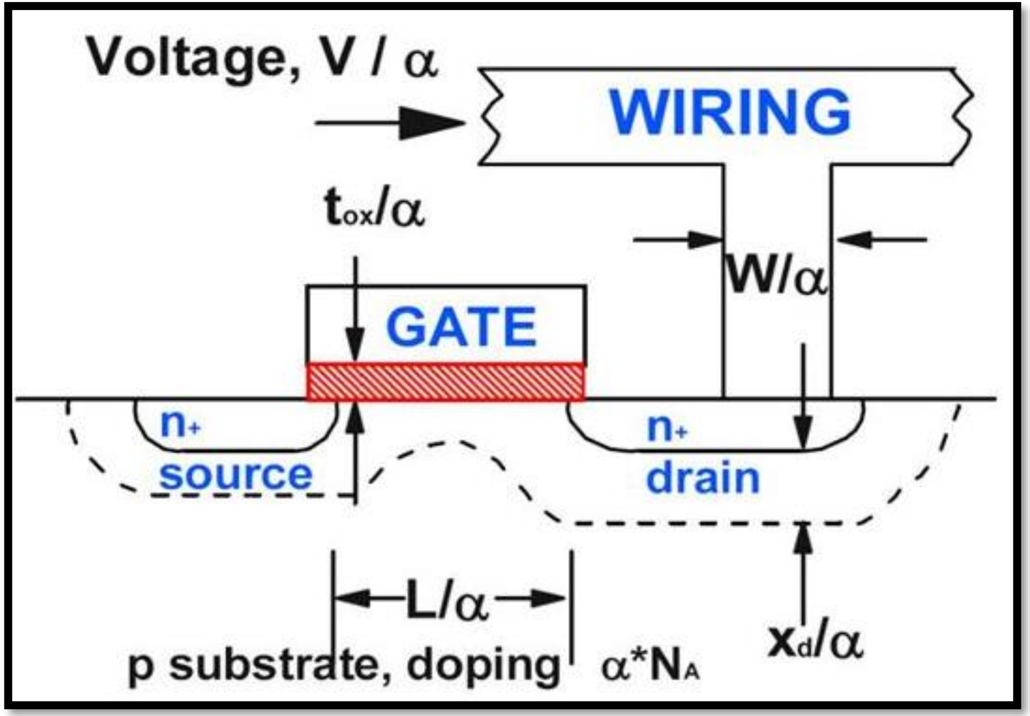


1975: # of transistors will double **every 2 years**

G. E. Moore, "Cramming more components onto integrated circuits", Electronics, vol. 38, no. 8, April 15, 1965.
G. E. Moore, "Progress in digital integrated electronics", IEEE IEDM Technical Digest, pp. 11-13, 1975.

Roadmap for MOSFET Scaling

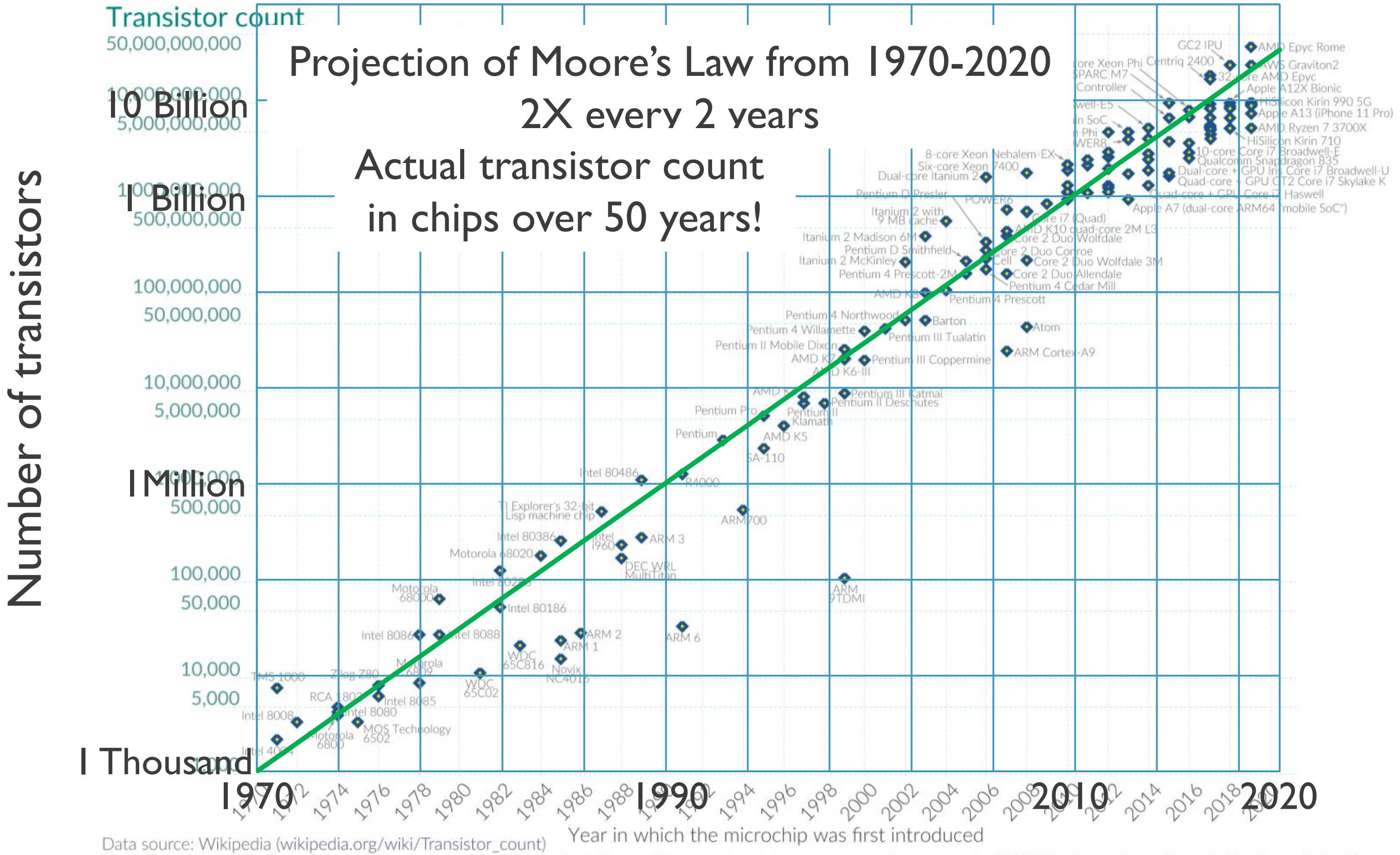
Robert Dennard, IBM



1974: Constant power scaling

R. Dennard et al., IEEE Journal of Solid State Circuits, vol. SC-9, no.5, pp. 256-268, Oct. 1974.

Number of Transistors in Chips Continue to Follow Moore's Law

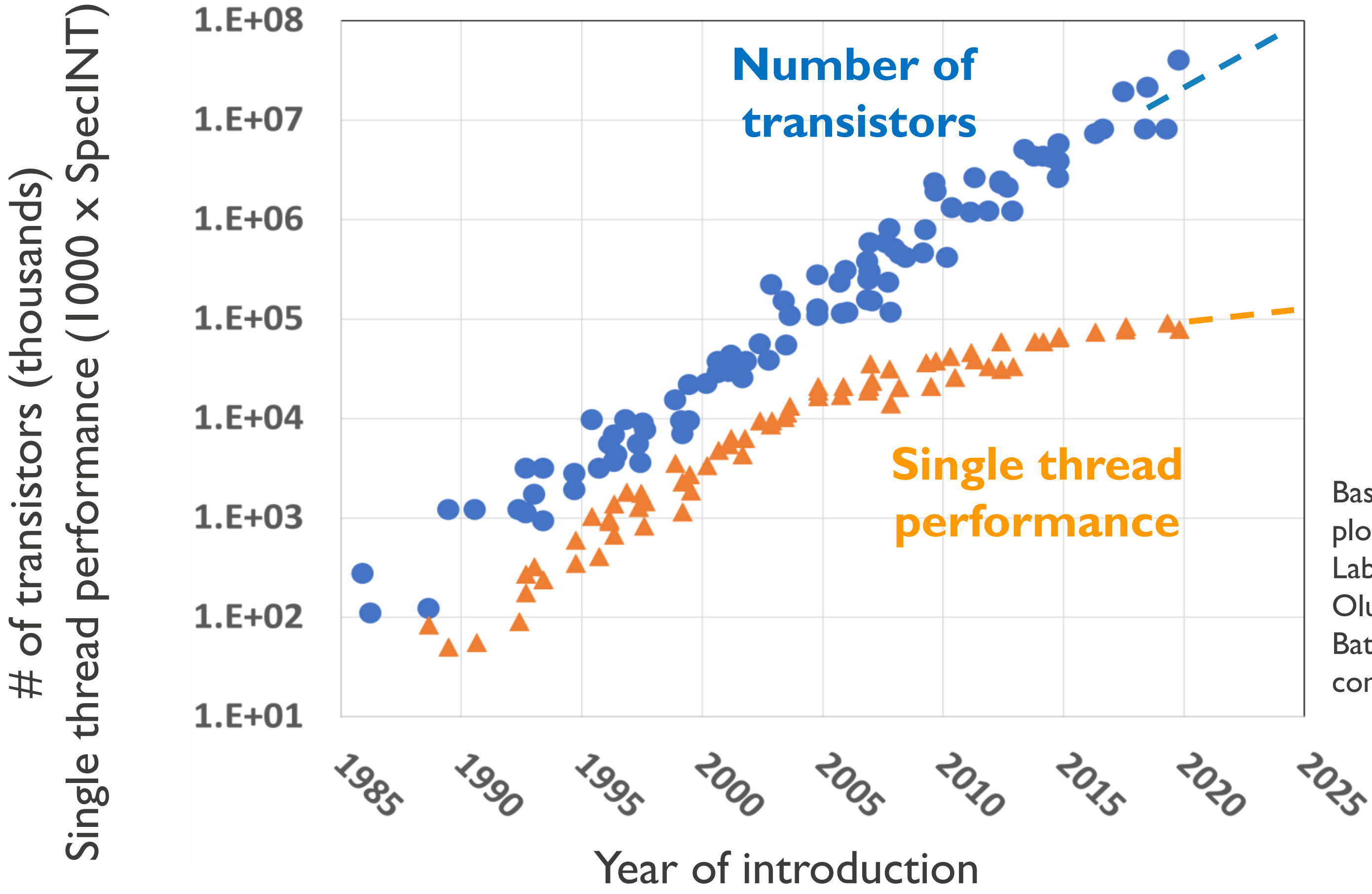


Projection of Moore's Law from 1970-2020
2X every 2 years

Actual transistor count
in chips over 50 years!

Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)
OurWorldinData.org – Research and data to make progress against the world's largest problems.

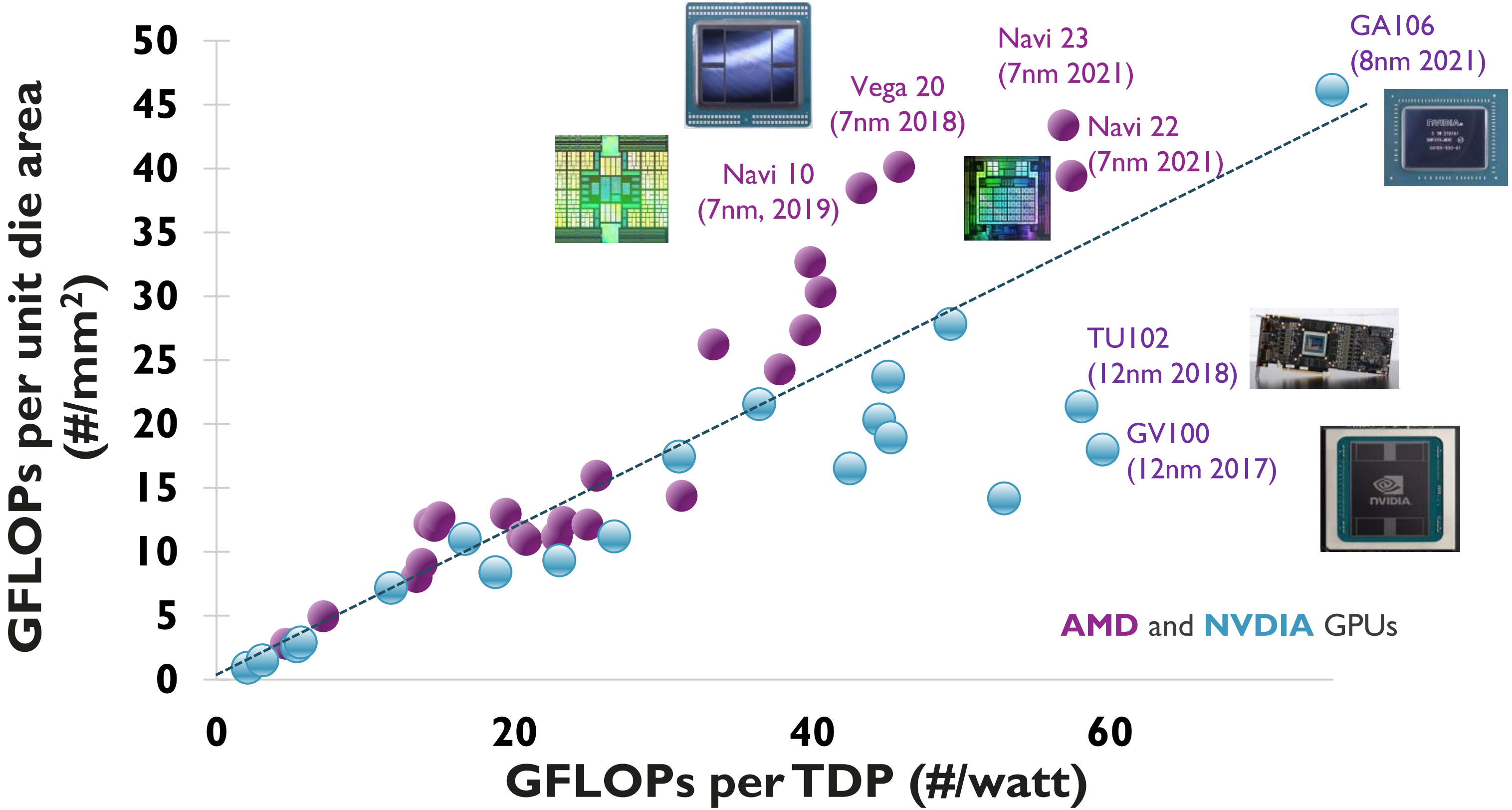
Scaling and Performance of General Purpose Compute (CPUs)



Based on original data plotted by M. Horowitz, F. Labonte, O. Shachan, K. Olukotun, L. Hammond, C. Batten. Additional data compiled by K. Rupp

Performance of Domain Specific Compute

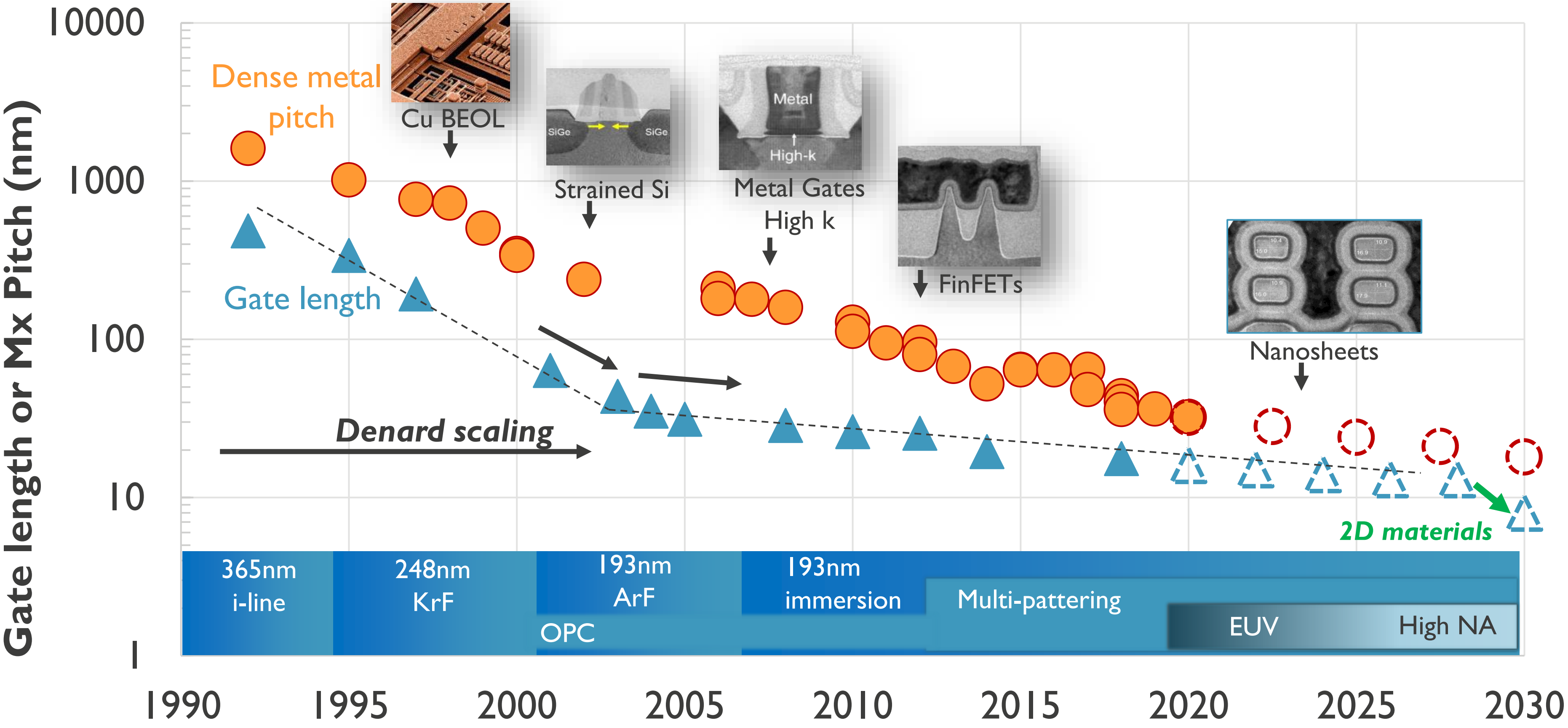
GPUs, NPUs continue to improve in area/power efficiency



Source: www.techpowerup.com/gpu-specs/

CMOS Technology Evolution

AIDED BY LITHOGRAPHY AND PROCESS INNOVATIONS



Includes data from: Michael L. Rieger, J. Micro/Nanolith. MEMSMOEMS18(4), (2019)

public

What Did the Chip Scaling Enable....

1956: IBM 350 Disk File
>1,000 Kg, 5MB storage

2021: USB drives
15g, 2TB storage

source: https://proftomcrick.com/2011/12/26/in-1956-5mb-was-big-enough-for-anyone/

What Did the Chip Scaling Enable....

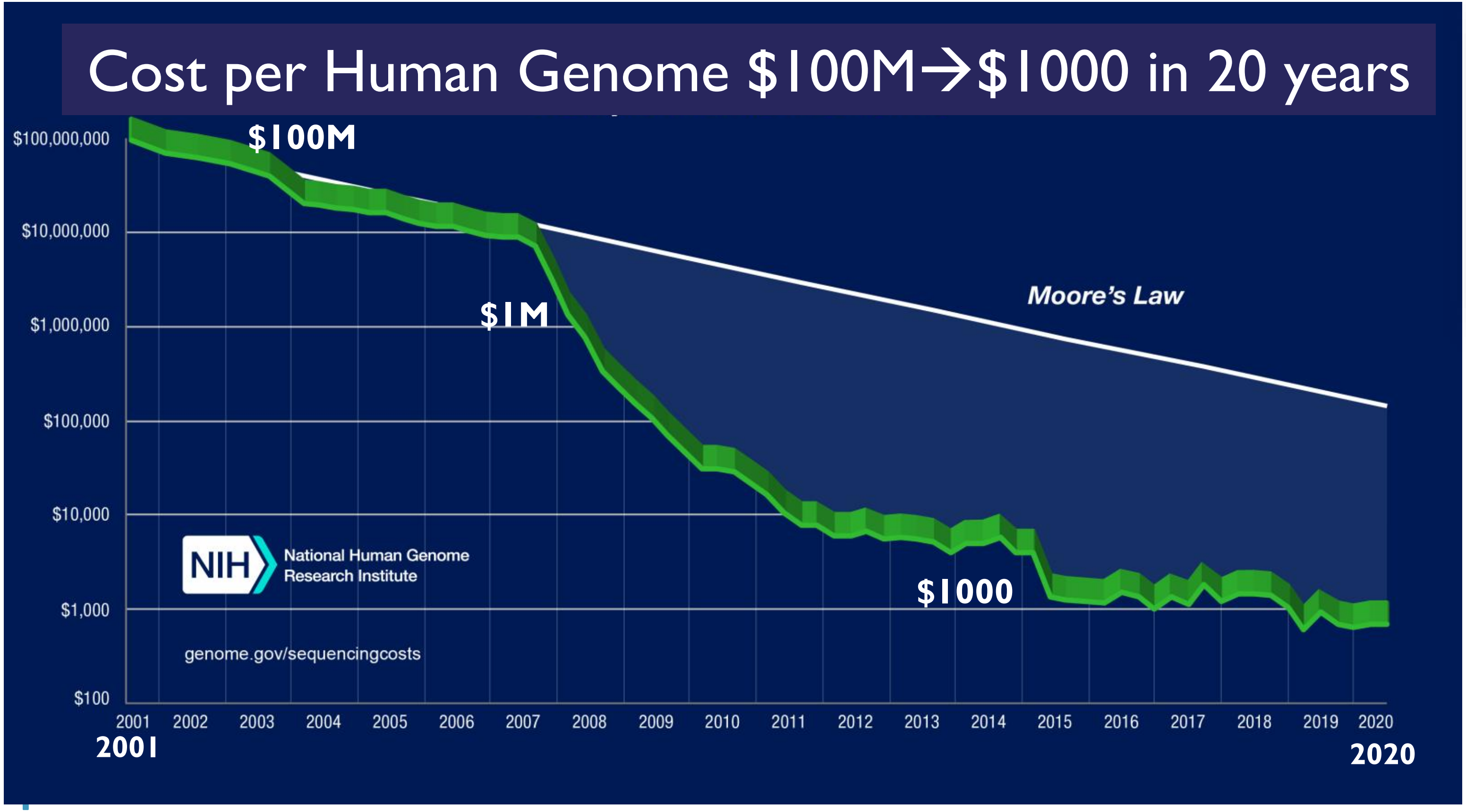

1990s


2020

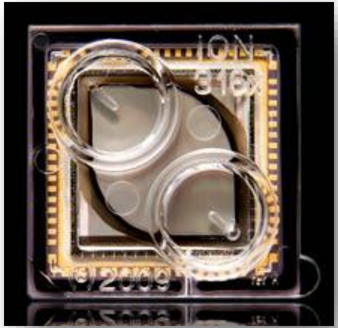
Images: Wikipedia and other sites

How Do Chip Innovations Impact our Lives?

Rapid Advances in DNA Sequencing, Drug and Vaccine Development



Cost per Human Genome $100M→$1000 in 20 years

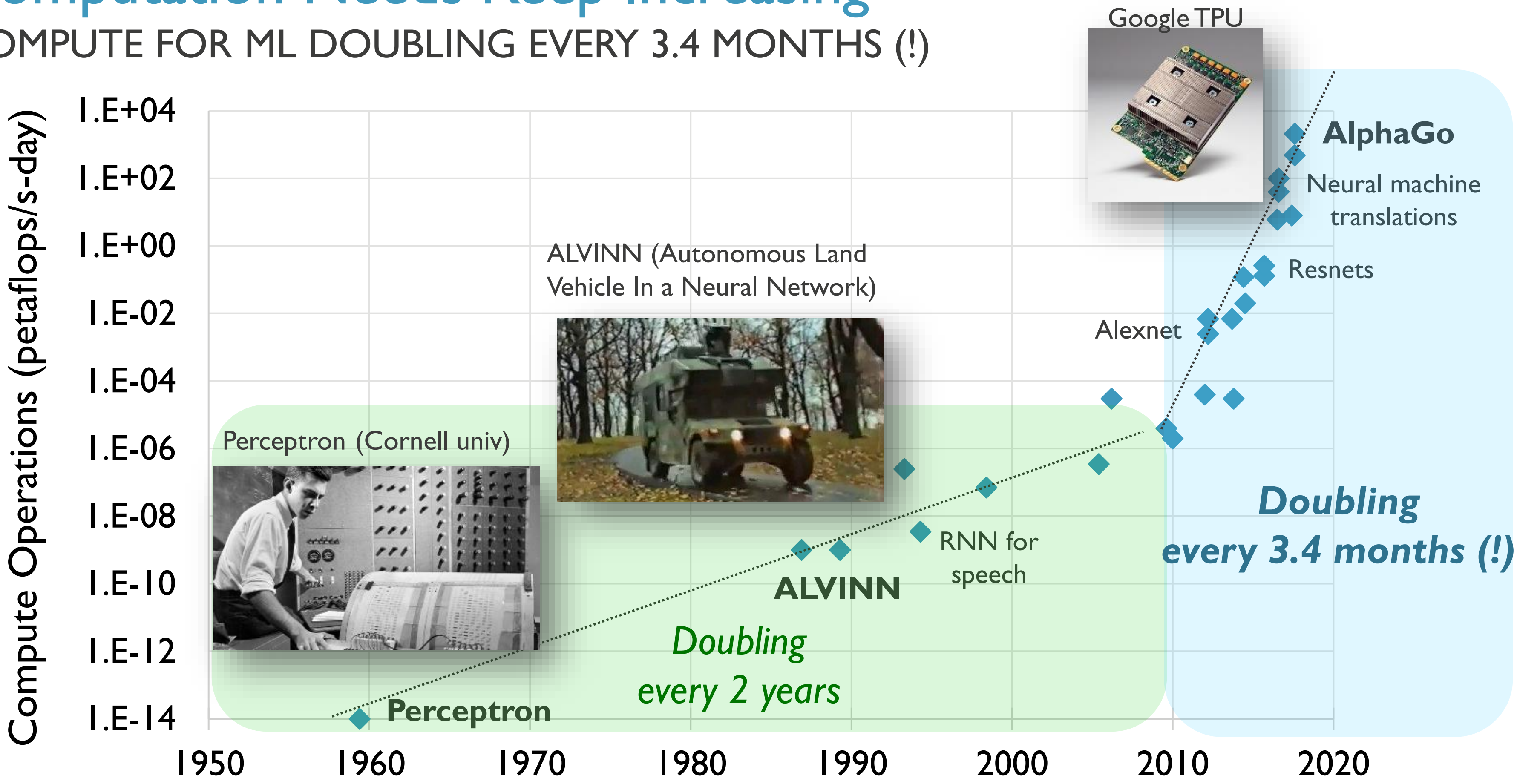


Ion Torrent's DNA sequencing chip, 2011

https://www.technologyreview.com/2011/07/21/192858/a-semiconductor-dna-sequencer/

Computation Needs Keep Increasing

COMPUTE FOR ML DOUBLING EVERY 3.4 MONTHS (!)



Data source: https://openai.com/blog/ai-and-compute/

Chips for Future Systems

High Performance

Mobile

Edge

Dimensional Scaling

New Materials

System Technology Co-optimization

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EUV Litho Roadmap Critical for Logic Scaling

Industry Timeline	**2024**	**2025**	**2026**	**2027**	**2028**	**2029**	**2030**	**2031**	**2032**

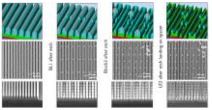
2nm
PP:42-45, MP: 20-22

A14
PP: 40-44, MP: 17-19

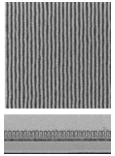
A10
PP: 38-42, MP: 15-17

A7 and beyond
PP: 36-40, MP: 13-15

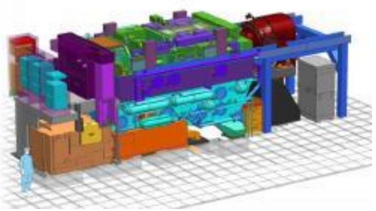
EUV 4th Gen
SAB, eSA(LE)^2 21nm



EUV 5th Gen
eSADP/eSA(LE)^2 18nm



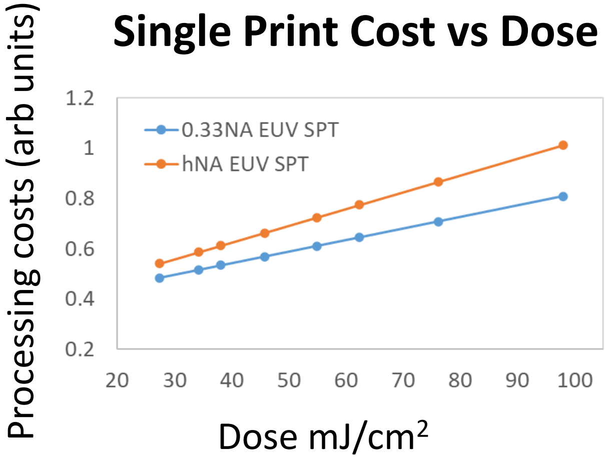
hNA EUV



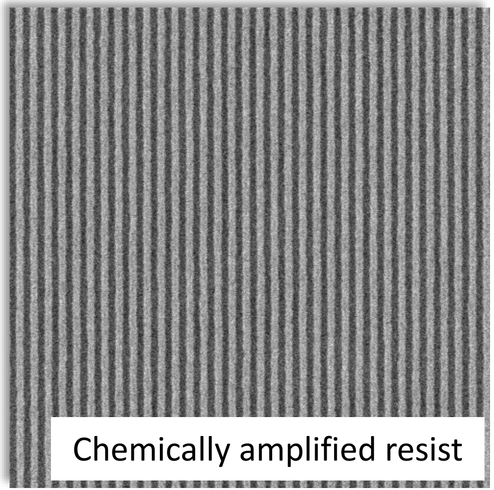
- Multi-patterned EUV (<28nm pitch) increases complexity and cost
    - New resists and patterning schemes to reduce dose (cost) and defectivity
- High NA EUV will provide some relief in cost, yield and cycle-time

PP: poly pitch (nm)
MP: dense metal pitch (nm)

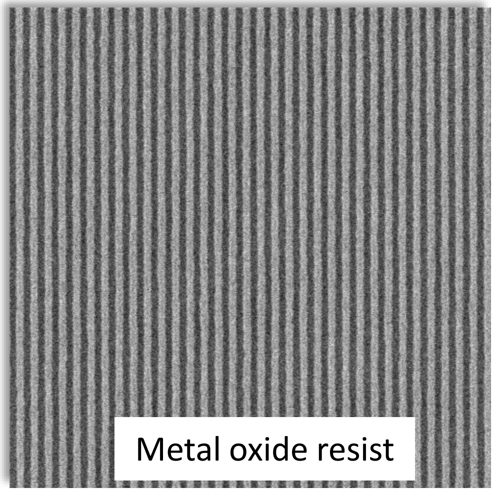
Need Focus on EUV Patterning Costs



28nm Pitch Single Expose EUV Patterning



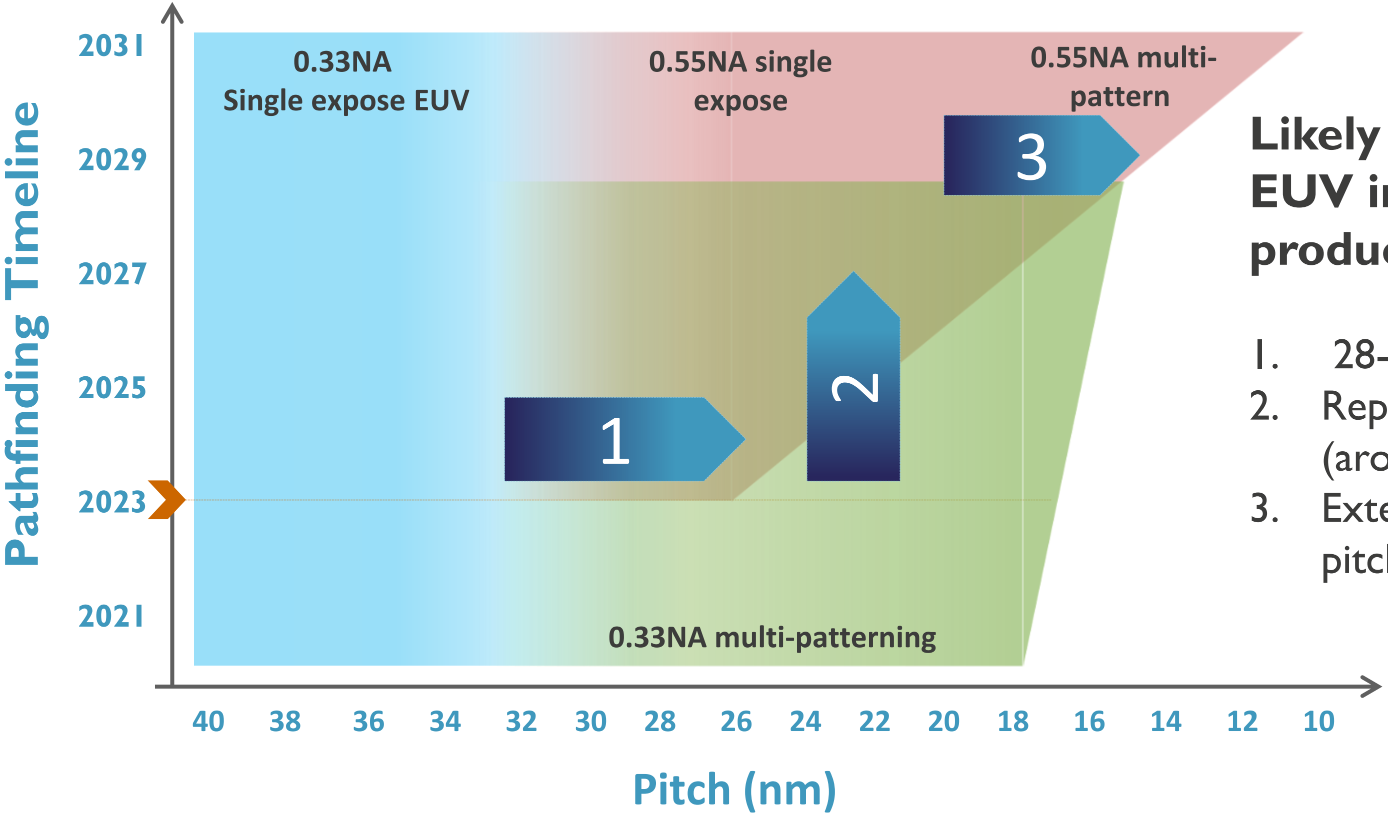
Dose: 61mJ/cm^2
CD: 14.5nm



Dose: **38.8mJ/cm^2**
CD: 14.0nm

Pushing limits of single exposure and new resists for throughput and cost

EUV LITHOGRAPHY: PITCH SCALING ROADMAP



Likely sequence of high NA EUV introduction in production

1. 28-32nm pitch (0.33NA limit)
2. Replace 0.33NA multi-patterning (around 20-24nm)
3. Extend SE resolution to ≤18nm pitches

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Logic Scaling Device Roadmap

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2nm
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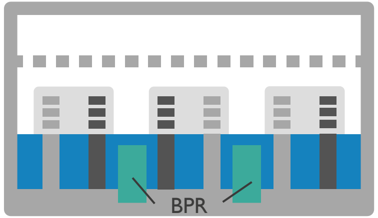
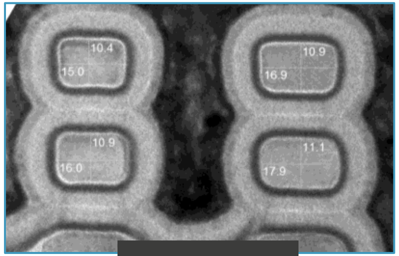
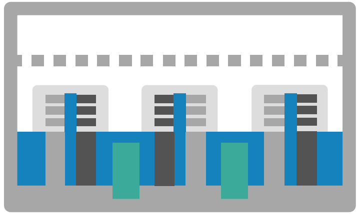


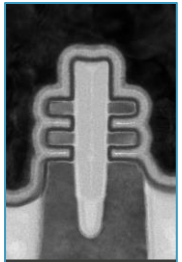
Nanosheets
→ **5T**



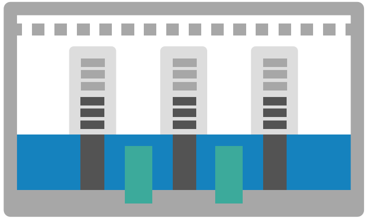
Nanosheets



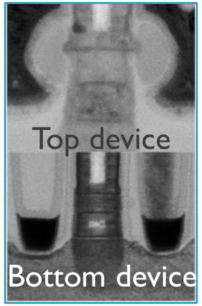
Forksheets
→**4T**

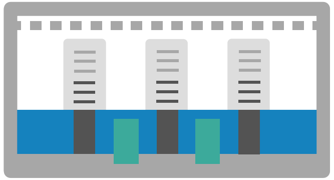


Forksheets



CFET
→**3T**





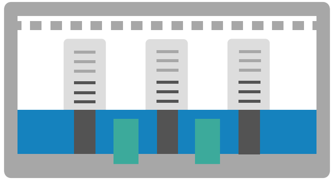
2D atomic channels

WS$_2$ 2D channel FET

PP: poly pitch (nm)
MP: dense metal pitch (nm)
CFET: Complementary FET

Computing Research Funnel Beyond 2D Channels

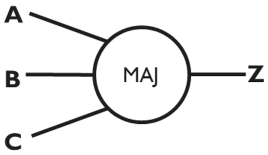
The next switch



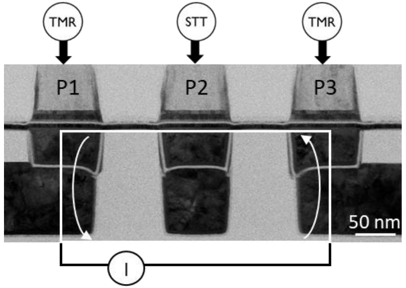
2D atomic channels

2D Atomic Channels

New Device Physics



Majority logic
could simplify circuits

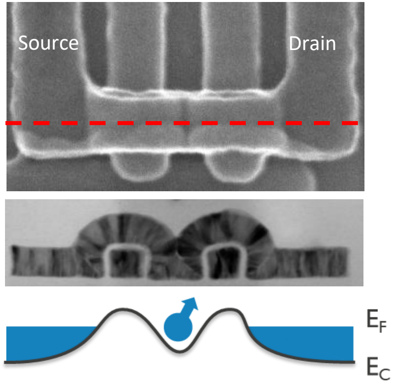


Logic w/ domain wall propagation by spin orbit torque between magnetic tunnel junctions

Spin Torque Majority Gates

Paradigm change

300mm Si spin qubit platform

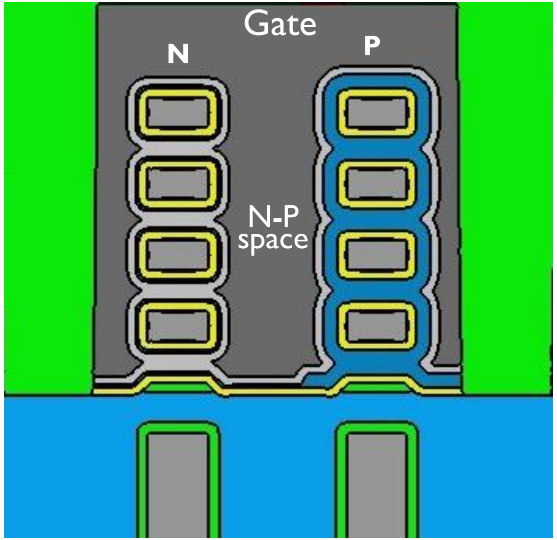


Qubit devices and electrical characteristic showing controllable particle occupation down to last e/ h

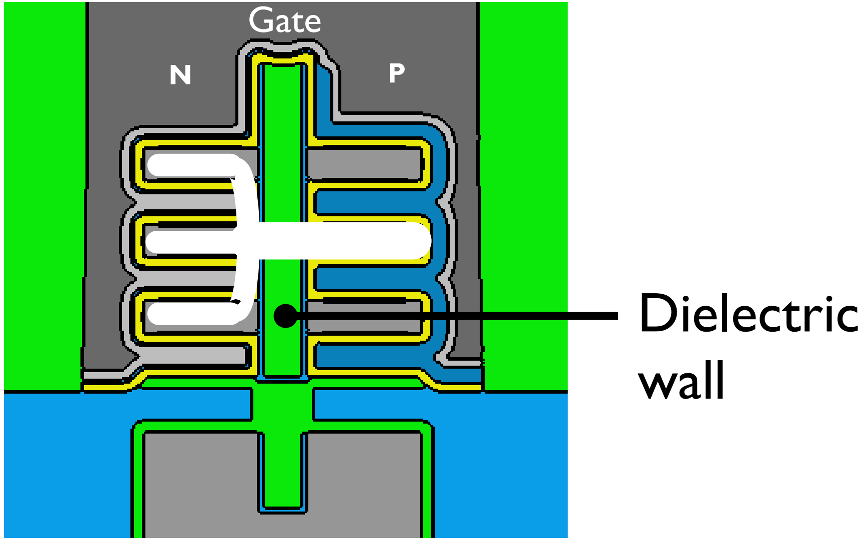
Quantum Computing

Forksheet: N-P space scaling

Nanosheet



Forksheet

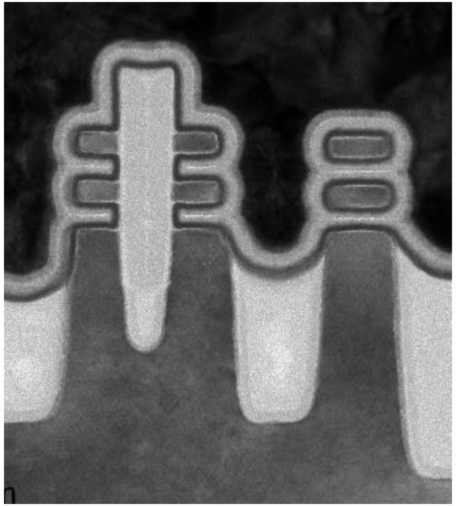


- Forksheets
  - Increase active width by reducing N-P space
  - Lower Miller and fringe capacitance→10% better performance

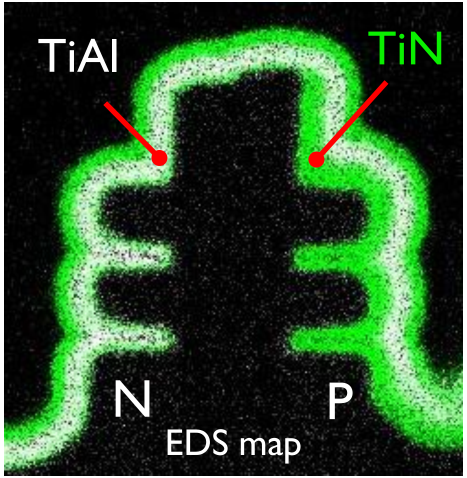
H. Mertens et al., VLSI 2021
P. Weckx et al., IEDM 2019

Forksheet-Nanosheet Co-integration

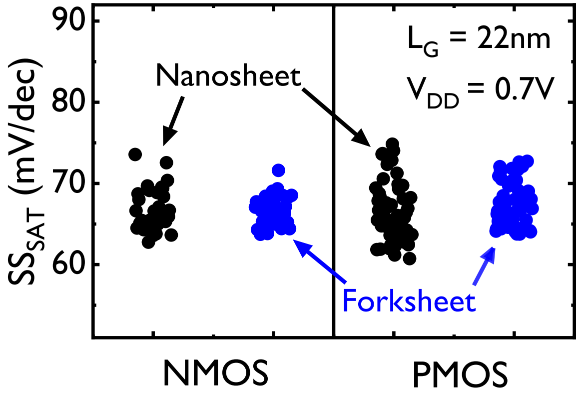
Forksheet-Nanosheet
co-integration



Dual work-function gates



SS



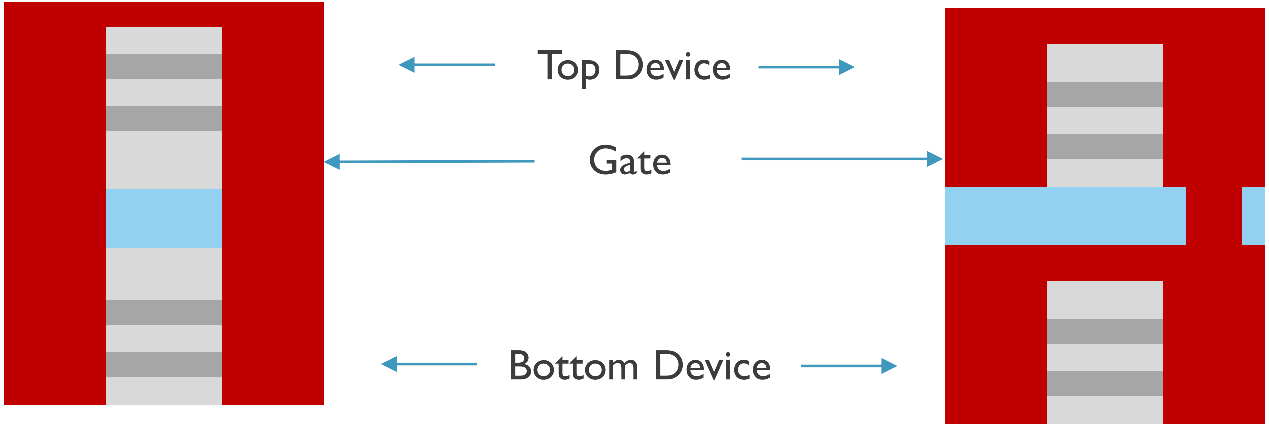
H. Mertens et al., VLSI 2021

1st Electrical demo of forksheet devices co-integrated with Nanosheets

Complementary FET (CFET)

MONOLITHIC CFET

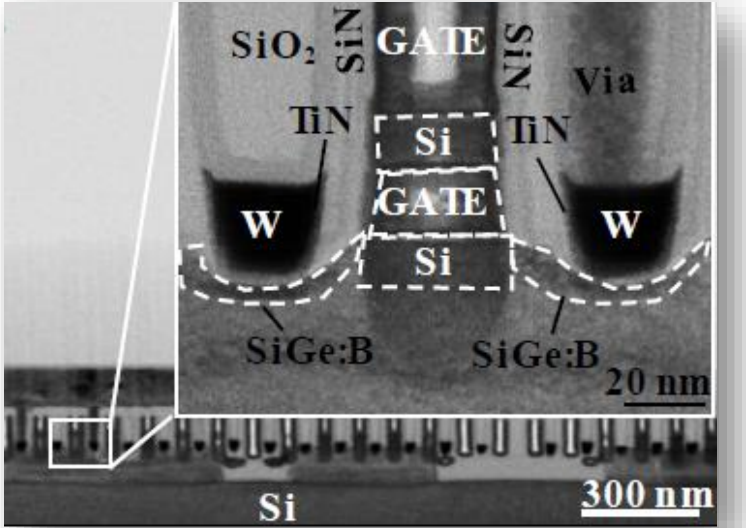
SEQUENTIAL CFET



Active areas and gates of top and bottom device **aligned**

Active areas and gates of top and bottom device **not aligned**

Complementary FET (CFET) Demonstrations



Monolithic Approach

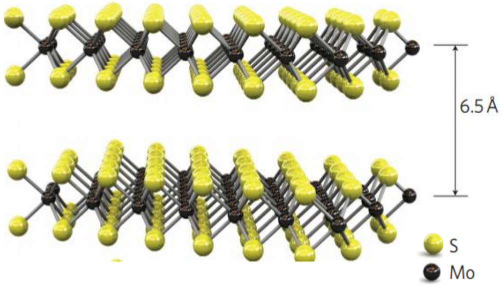
S. Subramanian, VLSI 2020

Sequential Approach

W. Rachmady, IEDM, 2019

- Many integration challenges with both approaches
- Sequential CFETs: different channel materials or orientation

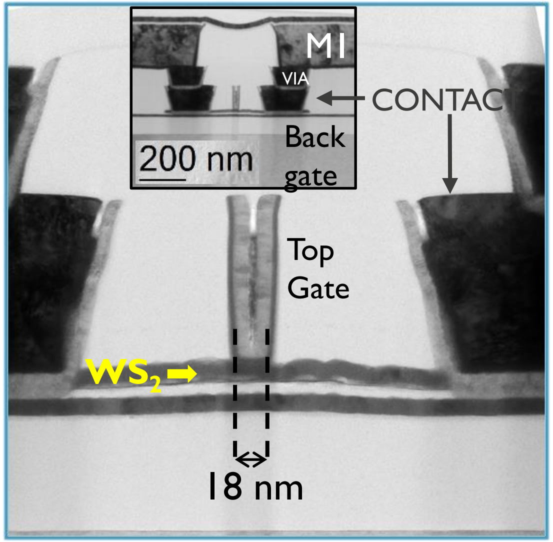
2D Atomic Channels: Next Gen Logic Devices



MoS_2

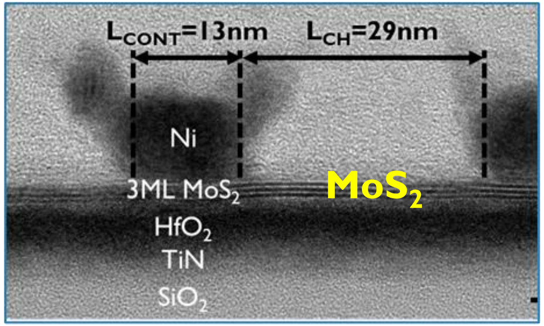
Monolayer channel thickness enables gate length scaling

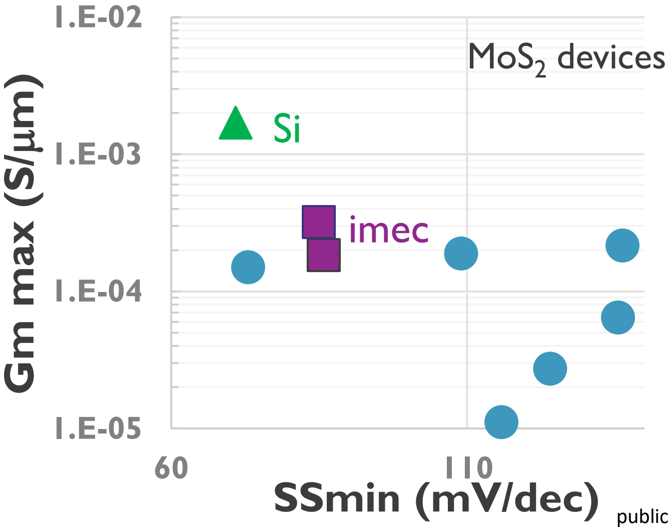
300mm Flow



I. Asselberghs et. al. IEDM 2020

Lab Flow





- Early demonstrations and promise
- Need significant improvements in mobility, contact resistance, gate dielectric scaling

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BEOL Scaling Roadmap

Optimizing resistance and capacitance

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2nm
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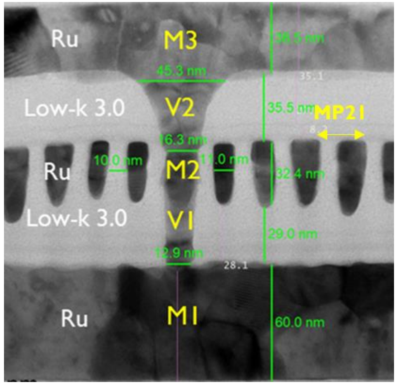
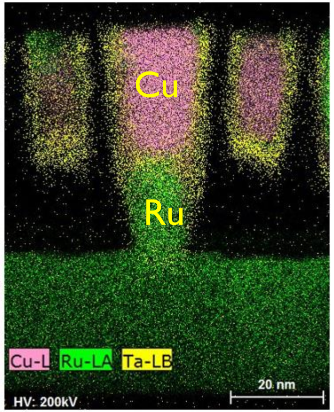
Dual-Damascene/Hybrid metallization

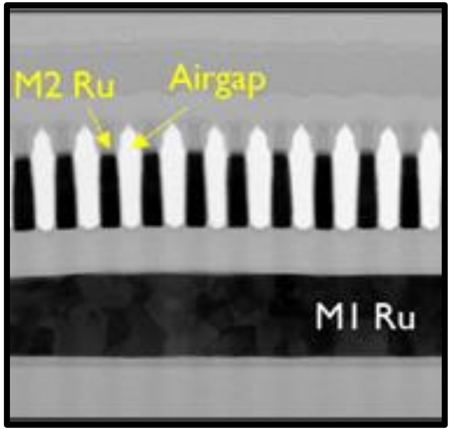
Semi-damascene (Subtractive metallization)



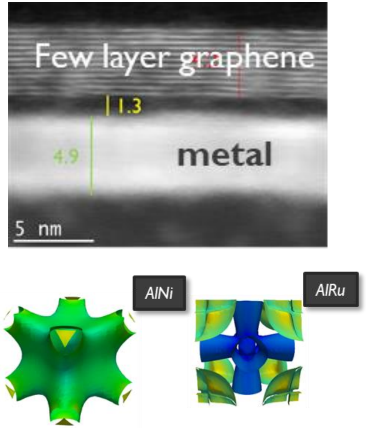
Dual-damascene 21nm pitch



Via resistance improvements



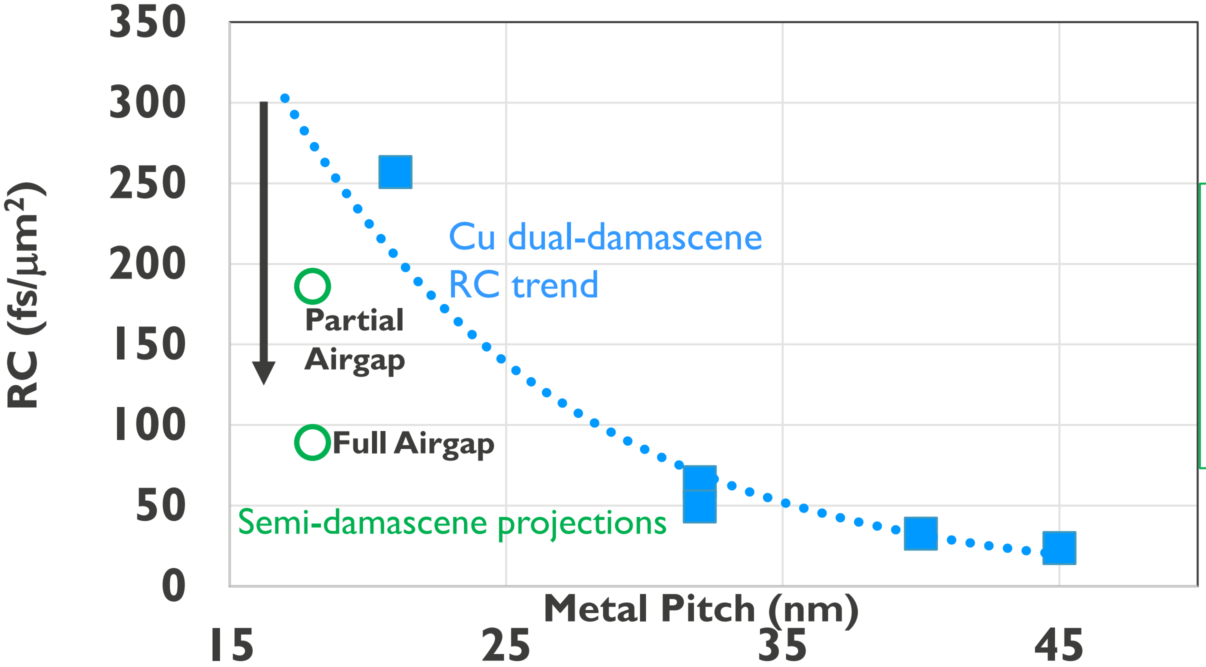
Direct metal etch w/ air-gaps



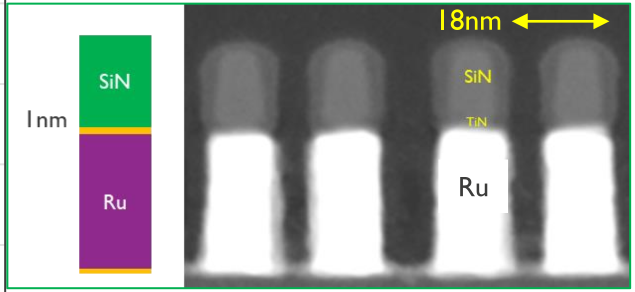
New metals to replace Copper

PP: poly pitch (nm)
MP: dense metal pitch (nm)

Semi-Damascene Integration to Address RC Challenge



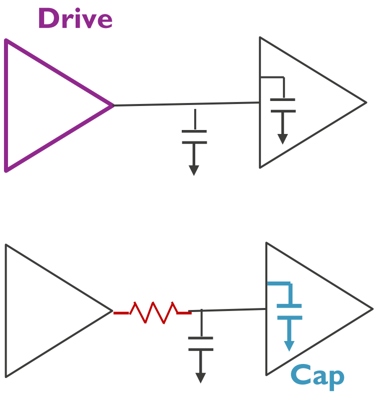
18nm Pitch Ru Etch



- Direct metal etch for high aspect ratio lines to lower resistance
- Partial or full air-gap to mitigate capacitance increase

Impact of Rapid BEOL Resistance Increase

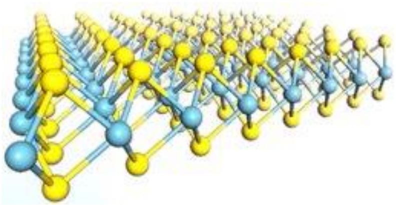
$$\text{Speed} \sim \frac{\text{Drive}}{\text{Cap}}$$



Historically higher FEOL drive improves speed

When BEOL R dominates then lower FEOL cap will improve speed

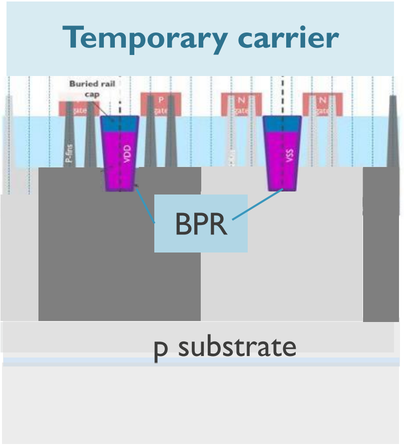
2D channels

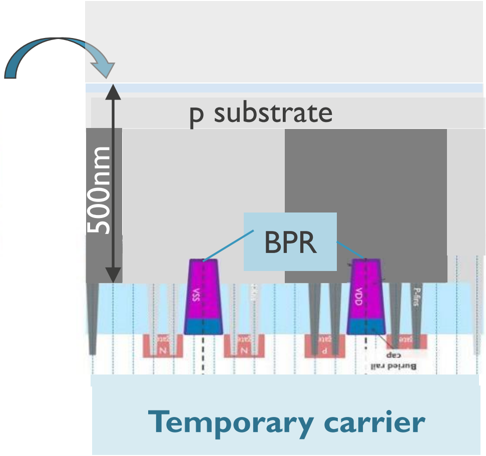


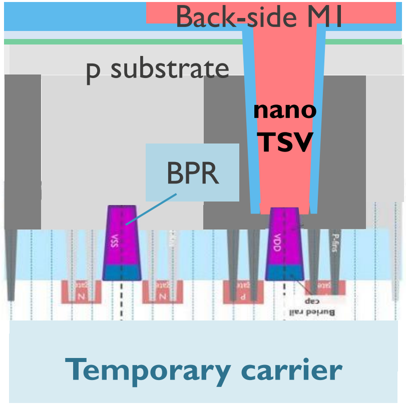
Ultra-thin Si

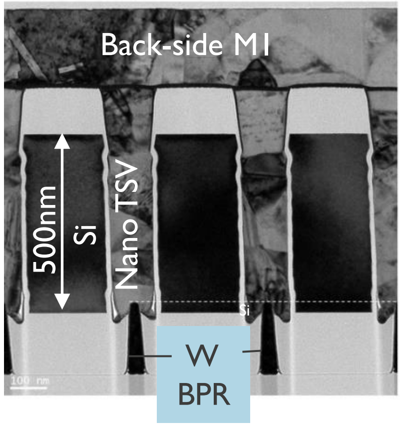
In scaled technologies where BEOL R dominates, devices with low FEOL cap will prevail

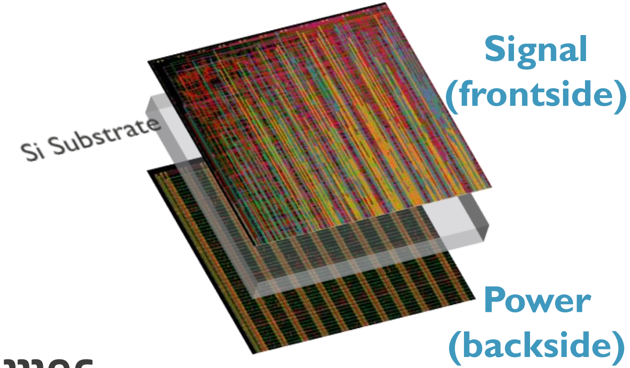
Wafer Backside Power Delivery Network (PDN)











- Nano TSV landing on BPR through thin Si back-side can enable power distribution
- Additional devices (ESD, MIMCAPs) on backside possible

BPR: Buried Power Rail

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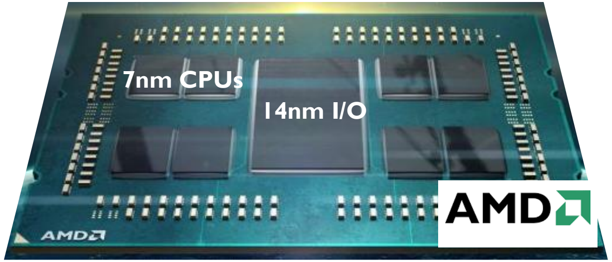
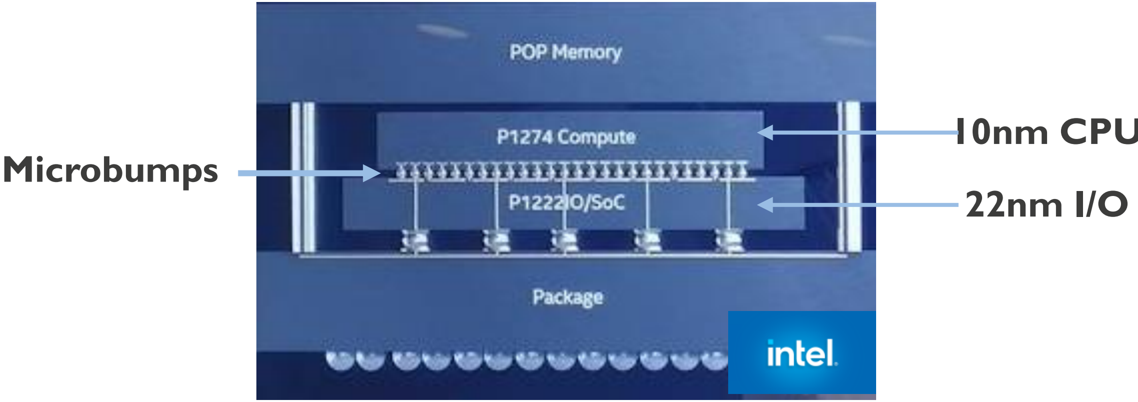
Examples of STCO at SoC Level

Partitioning of Chips for Power-Performance-Area-Cost



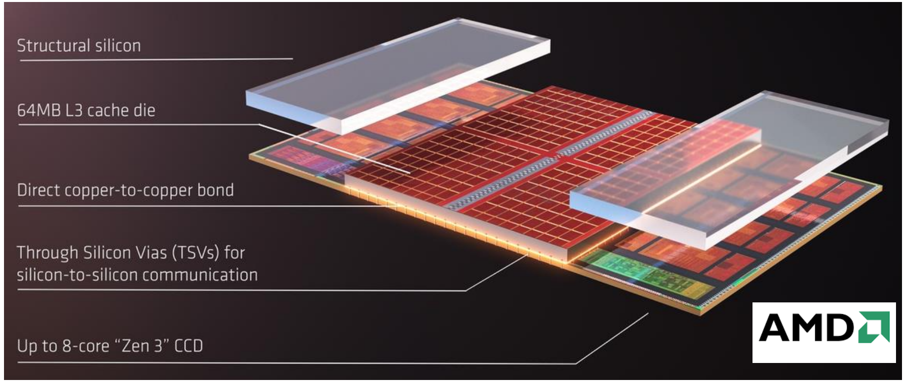
AMD Epyc Chiplet Architecture, **2019**

Drivers: Yield, cost



Intel Foveros Lakefield Hybrid CPU, **2020**

Drivers: Form factor, power



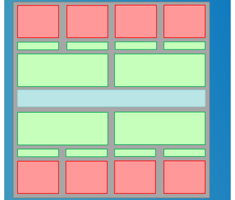
AMD 3D V-cache (added L3 cache SRAM on CPU), **2021**

Driver: Performance

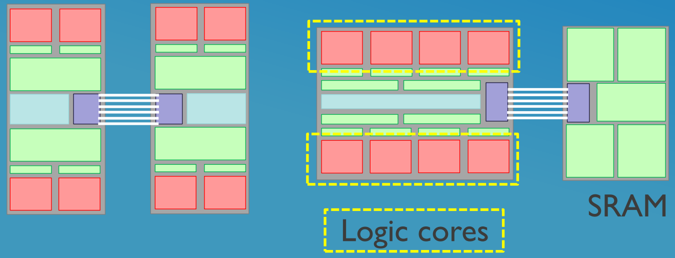
3D SoC Partitioning of Memory-logic

Addressing the memory wall issue

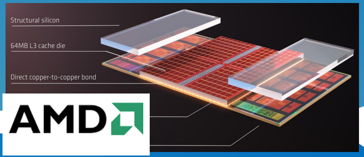
2D-SOC



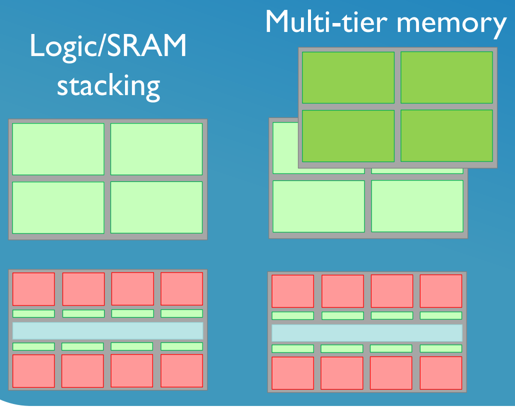
Chiplet Approach



- **Communication**: *interface bus protocol*
- **Design**: separate chips
- **Partitioning**: last level cache only
- **Examples**: AMD 3D V-cache

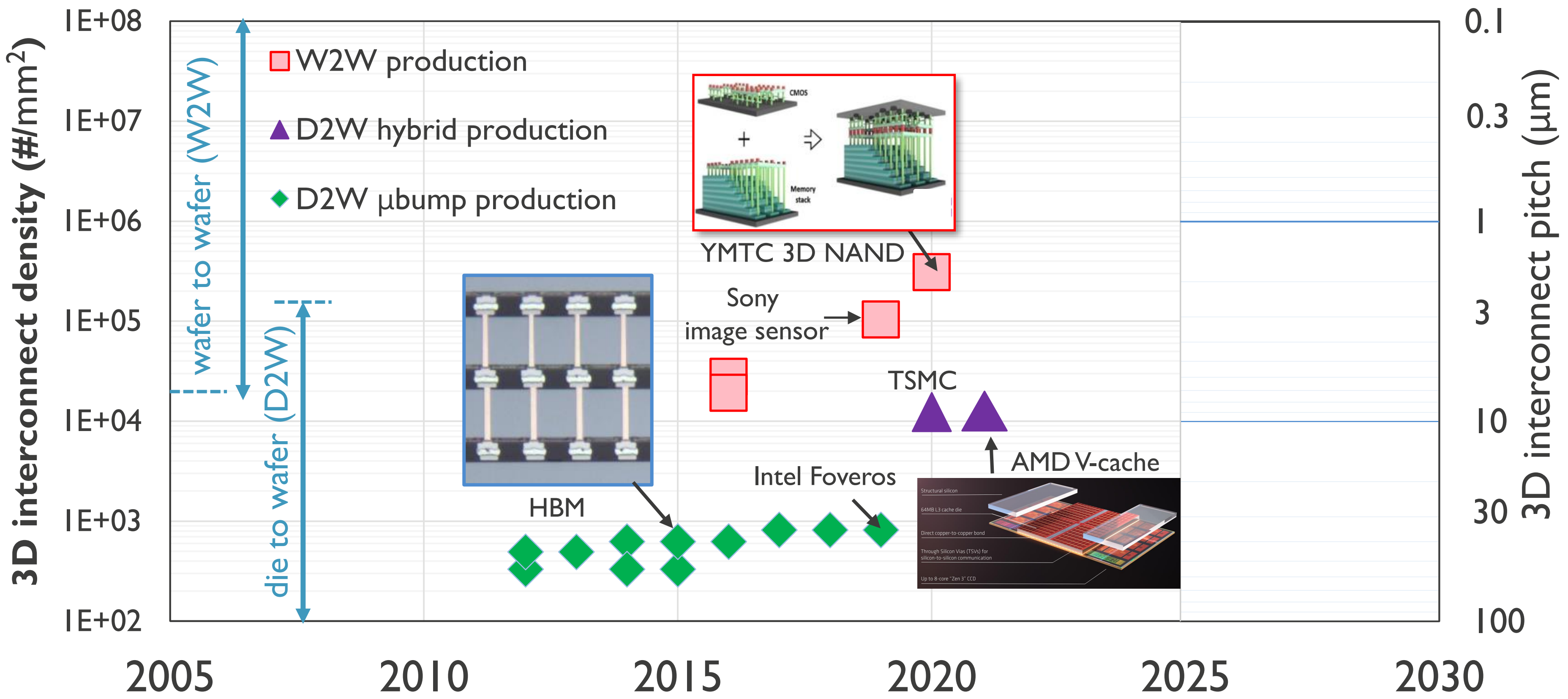


3D SoC Co-design



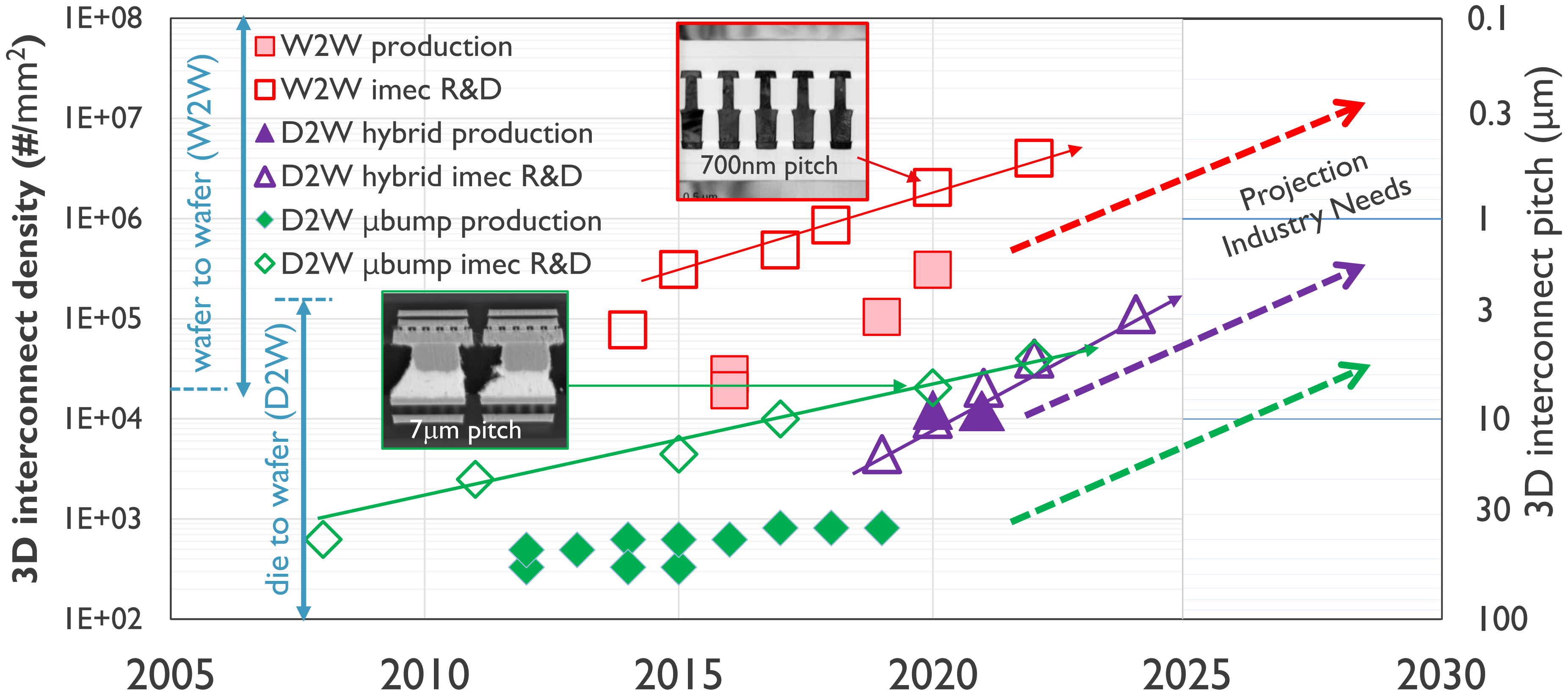
- **Communication**: *Direct communication*
- **Design**: simultaneous co-design→ needs 3D EDA enablement (!)
- **Partitioning**: Lower level caches also
- **Integration**: need high density 3D interconnects

3D Interconnect Technologies in Production



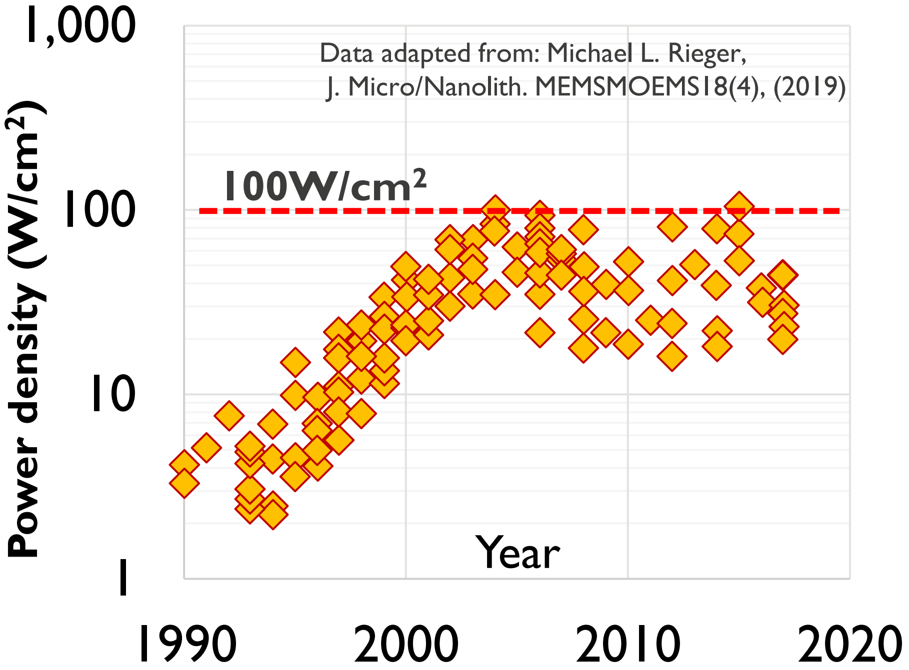
Includes data from H.-S. P. Wong et al., "A Density Metric for Semiconductor Technology", Proc. IEEE, vol.108, No.4, 2020 and Techinsights AME-2003-801.

3D Interconnect imec R&D Roadmap

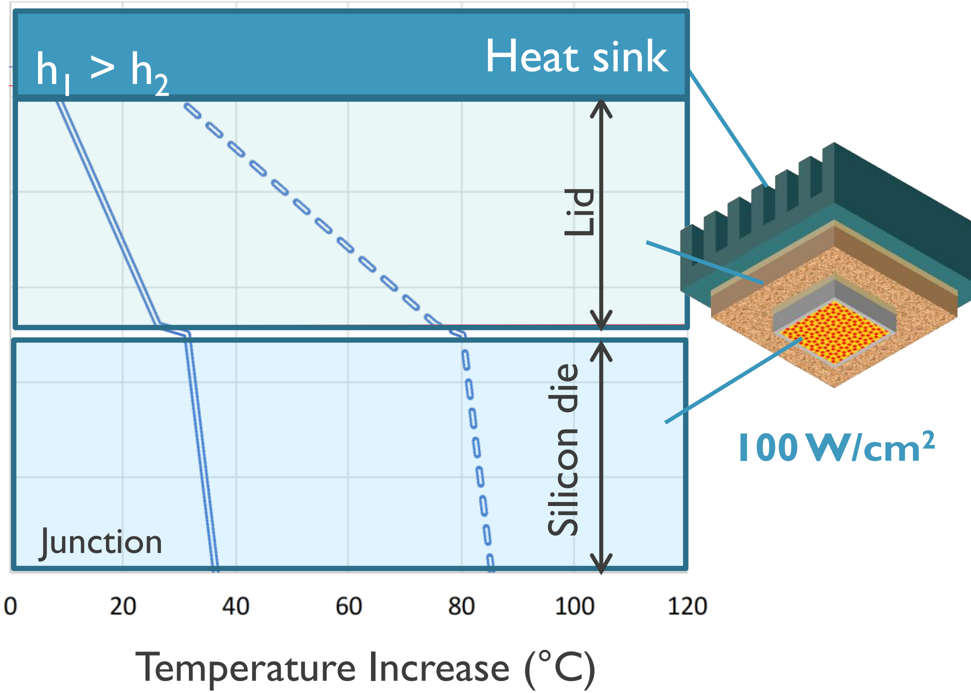


Includes data from H.-S. P. Wong et al., "A Density Metric for Semiconductor Technology", Proc. IEEE, vol.108, No.4, 2020 and Techinsights AME-2003-801.

Heat Removal in Stacked or Single Die



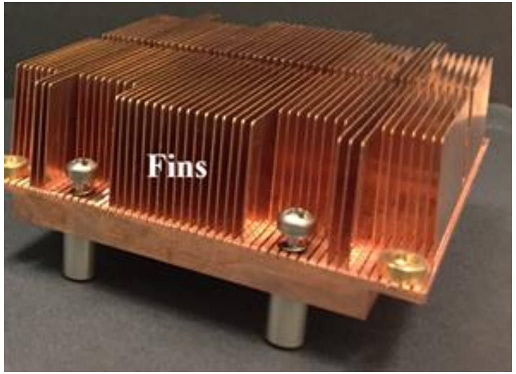
Data adapted from: Michael L. Rieger, J. Micro/Nanolith. MEMSMOEMS18(4), (2019)

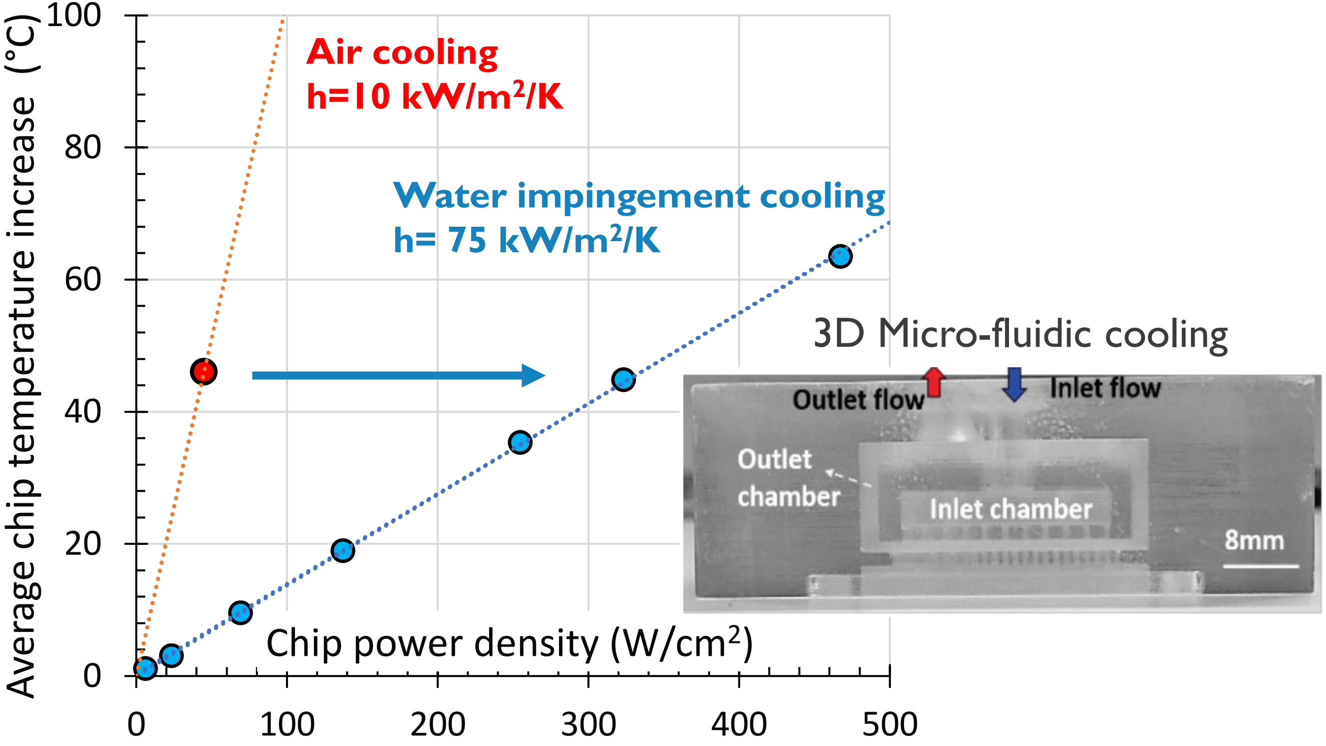


- Power wall ~100W/cm² limits system performance
- Thermal gradient in package lid determines junction temperature

Impingement Water Cooling on Bare Silicon Die

Standard air cooling





- Jet impingement water cooler enables high external heat transfer
- Can cool die with 200-400 W/cm^2 power densities

T. Wei et al., IEEE Trans. CPMT, DOI 10.1109/ TCPMT.2020.3045113

Outline

- Historical Perspective
- Advanced Patterning
- CMOS Devices
- BEOL Evolution
- System Technology Co-optimization
- **Environmental Impact of Logic Scaling**

Carbon Footprint of Semiconductor Manufacturing

The Chip Industry Has a Problem With Its Giant Carbon Footprint

Each new generation of semiconductors requires more energy, water and greenhouse gases to create.

Source: https://www.bloomberg.com/news/articles/2021-04-08

Carbon footprint
IC production is growing

2021

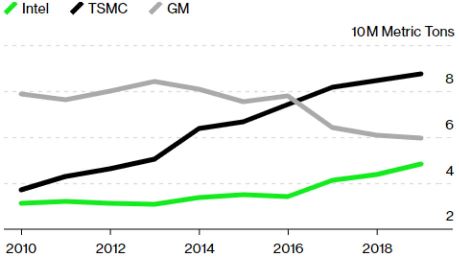
2030

System companies
Pledge to be carbon free

2040

Chip Producers Overtaking Automakers as Polluters

The environmental cost of semiconductors is rising



Source: Company disclosures
Note: Metric tons of green house gas emissions

"…Apple is carbon neutral. And by **2030**, all our products will be too…."

"…co-founded The Climate Pledge – a commitment to be net zero carbon across our business by **2040**…."

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Carbon footprint IC production is growing

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Increased impact from IC manufacturing, but uncertain projections

2030

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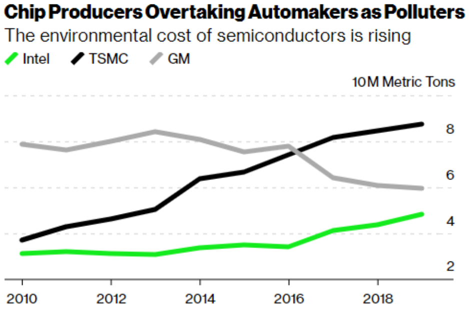

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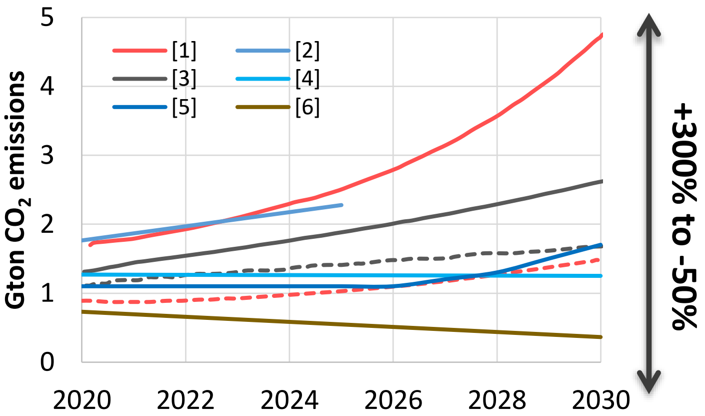
Greenhouse Gas emissions IC sector



[1] Andrae, et al. Challenges, 2015, 6, 117-157
[2] Bordage, F. The environmental footprint of the digital world online, 2019
[3] Belkhir et al., Journal of Cleaner Production, 2018, 177, 448-463
[4] #SMARTer2030 ICT Solutions for 21st Century Challenges online, 2015
[5] Andrae, A. S., Engineering and Applied Science Letter, 2021, 80-97
[6] Freitag et al., The climate impact of ICT: A review of estimates, trends and regulations 2021

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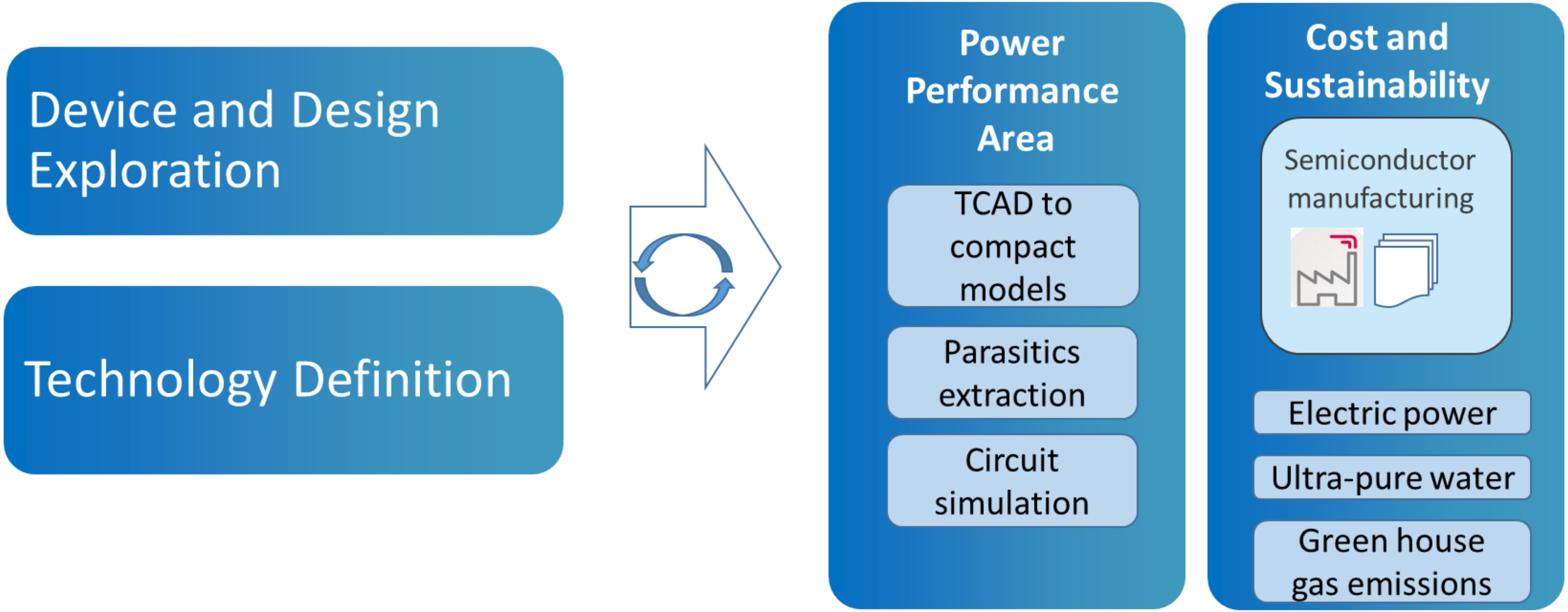
Environmental Impact of Logic Scaling

Framework to evaluate cost of technology choices



Device and Design Exploration

Technology Definition

Power Performance Area

TCAD to compact models

Parasitics extraction

Circuit simulation

Cost and Sustainability

Semiconductor manufacturing

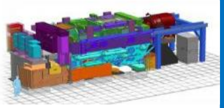
Electric power

Ultra-pure water

Green house gas emissions

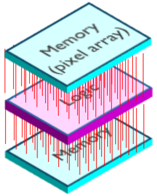
M. G. Bardon et. al., IEDM 2020

Takeaways: Future Logic Scaling



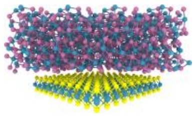
Dimensional scaling will continue

- High-NA EUV lithography
- New devices: Forksheets, CFETs



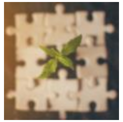
2D chips →3D chips

- Partitioning of chip functions: memory, back-side power
- EDA tools and 3D technologies need to mature



Focus on new materials

- 2D atomic channels
- New metals



Sustainable scaling

- Awareness and choices during pathfinding

Thank You

Acknowledgement

Our partners who support imec

and

all the imec researchers whose work I shared today